



Description

JMP N-channel Enhancement Mode Power MOSFET

Features

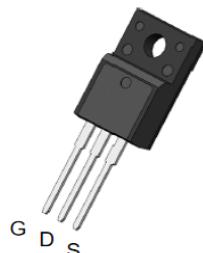
- 500V, 18A
- $R_{DS(ON)} < 0.36\Omega$ @ $V_{GS} = 10V$
- Fast Switching
- Improved dv/dt Capability

Applications

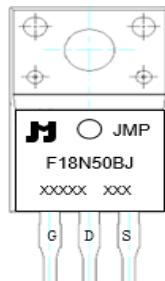
- Load Switch
- PWM Application
- Power Management



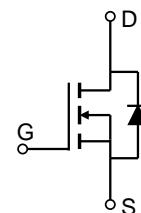
100% UIS TESTED!
100% ΔV_{ds} TESTED!



TO-220FP-3L Top View



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	TUBE (pcs)	Inner Box (pcs)	Per Carton (pcs)
JMPF18N50BJ	JMPF18N50BJ	TUBE	TO-220FP-3L	50	1000	5000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	500	V
V_{GS}	Gate-to-Source Voltage	± 30	V
I_D	Continuous Drain Current $T_C = 25^\circ C$	18	A
		11	
I_{DM}	Pulsed Drain Current ⁽¹⁾	72	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	708	mJ
P_D	Power Dissipation $T_C = 25^\circ C$	34	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	49	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$



Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	500	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 30\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	3	4	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 9\text{A}$	-	0.28	0.36	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$	-	2839	-	pF
C_{oss}	Output Capacitance		-	258	-	pF
C_{rss}	Reverse Transfer Capacitance		-	28	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 250\text{V}, I_D = 18\text{A}$	-	58	-	nC
Q_{gs}	Gate Source Charge		-	16	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	19	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 243\text{V}$ $I_D = 18\text{A}, R_{\text{GEN}} = 24\Omega$	-	41	-	ns
t_r	Turn-On Rise Time		-	53	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	168	-	ns
t_f	Turn-Off Fall Time		-	62	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	18	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	72	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 18\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 18\text{A}, di/dt = 100\text{A/us}$	-	423	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	5.5	-	μC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=10\text{mH}$, $I_{AS}=12\text{A}$

3. $R_{\theta JA}$ is measured with the device mounted on a minimum recommended pad of 2oz copper FR4 PCB

4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

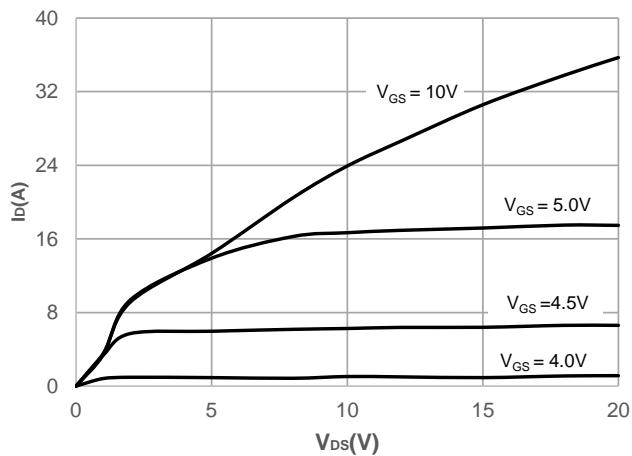


Figure 2: Typical Transfer Characteristics

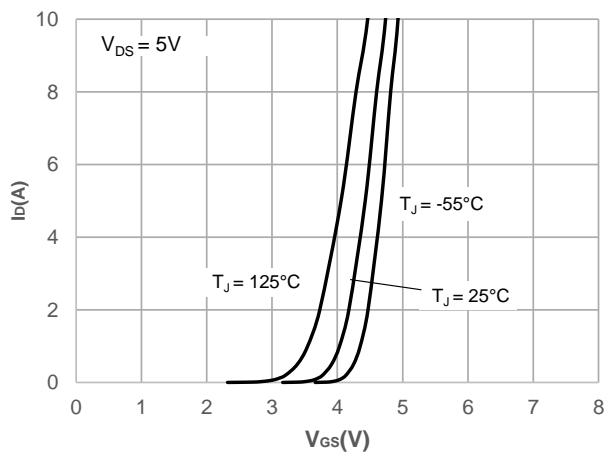


Figure 3: On-resistance vs. Drain Current

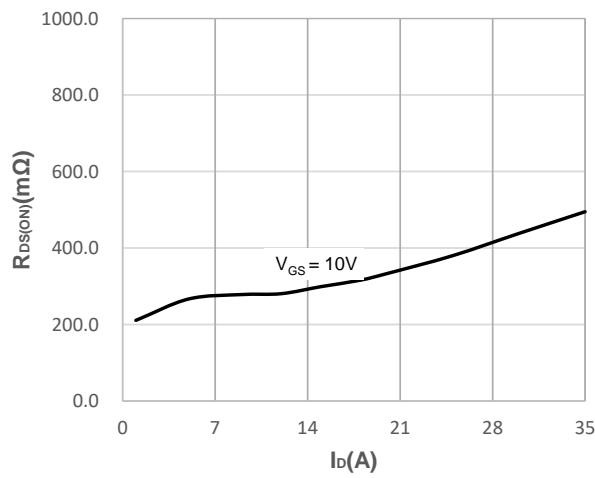


Figure 4: Body Diode Characteristics

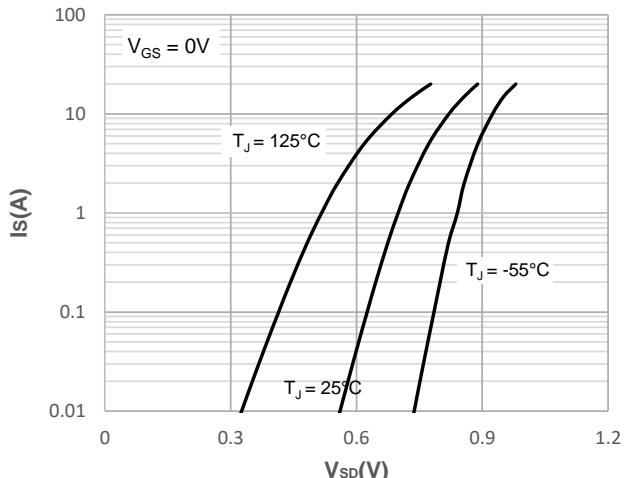


Figure 5: Gate Charge Characteristics

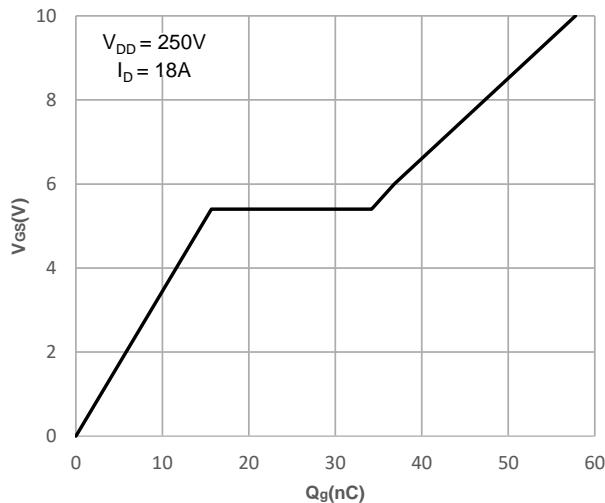
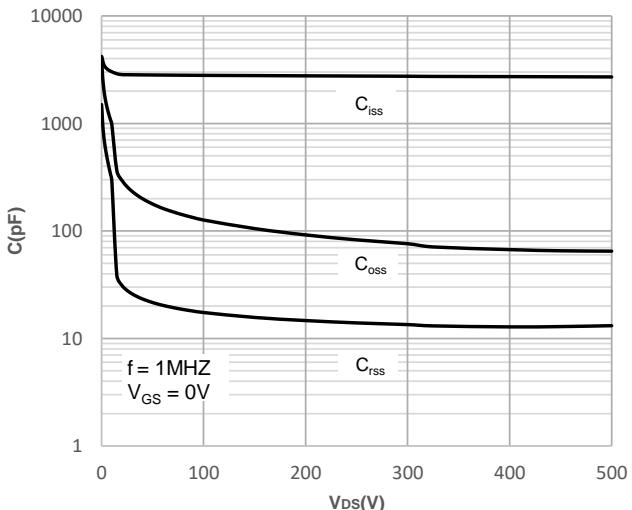


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

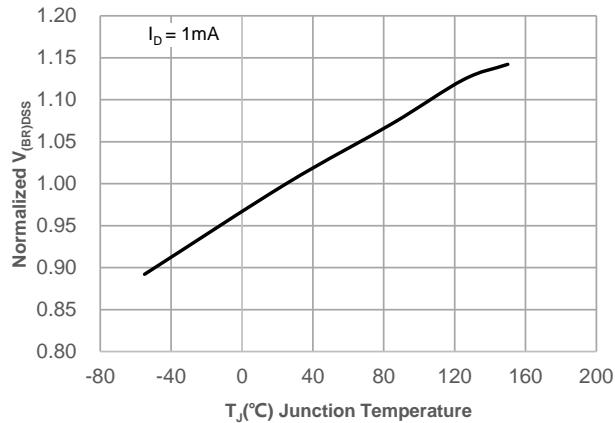


Figure 8: Normalized on Resistance vs. Junction Temperature

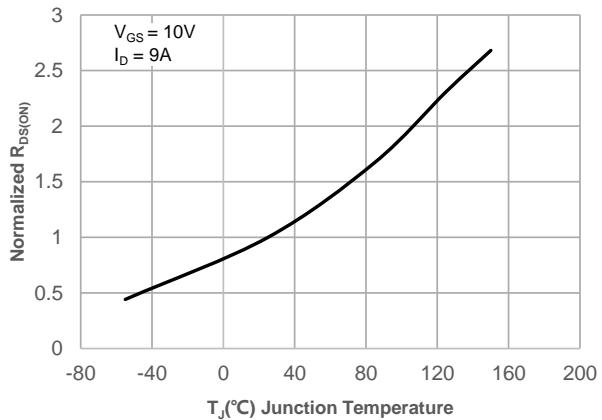


Figure 9: Maximum Safe Operating Area

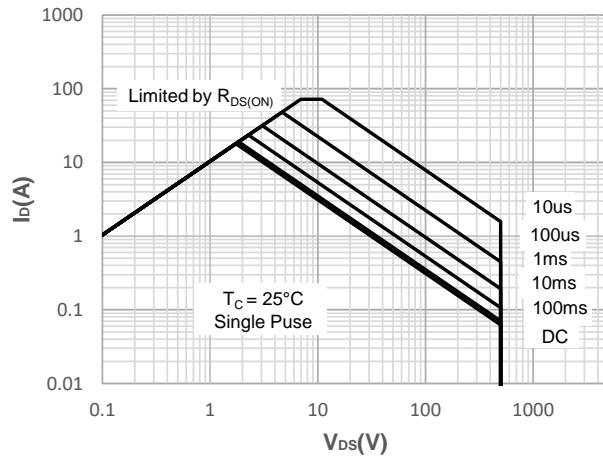


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

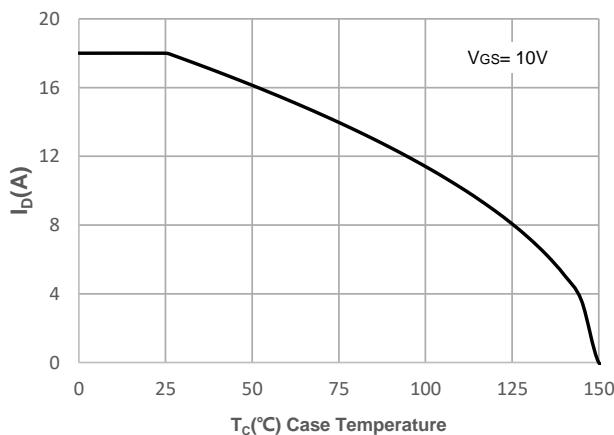


Figure 11: Normalized Maximum Transient Thermal Impedance

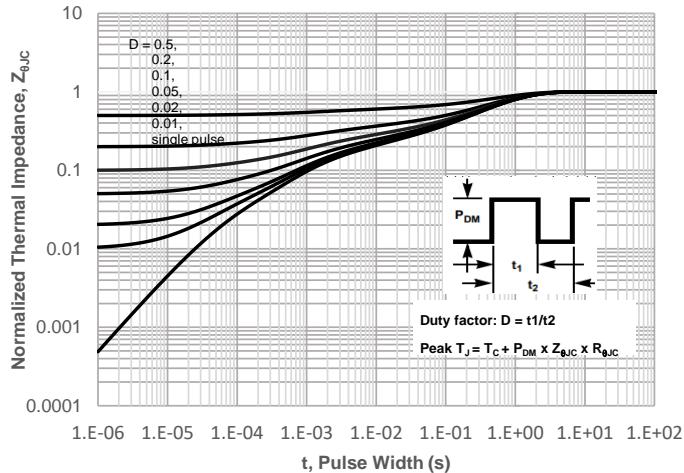
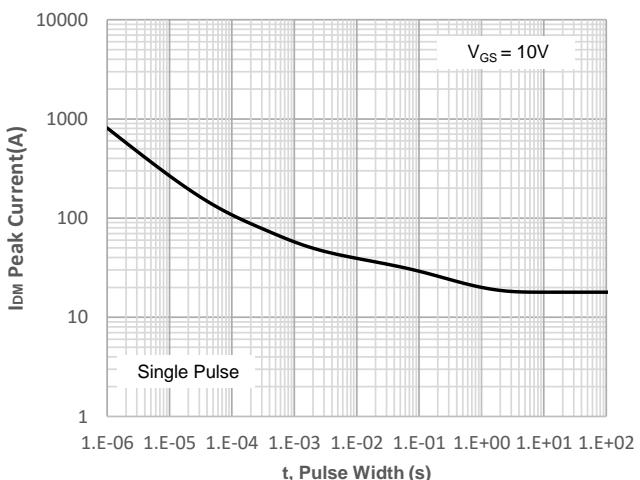


Figure 12: Peak Current Capacity



Test Circuit

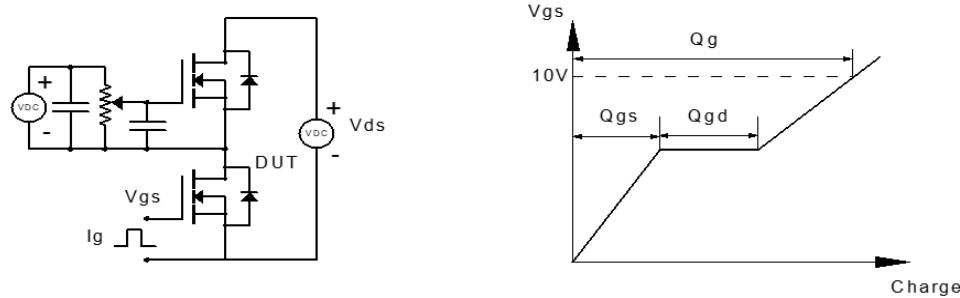


Figure 1: Gate Charge Test Circuit & Waveform

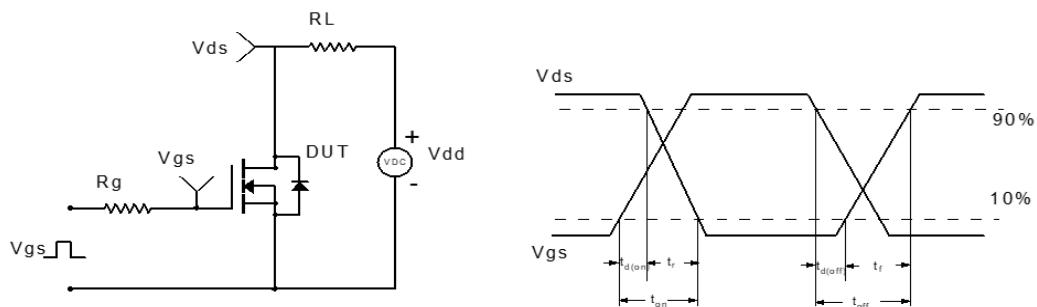


Figure 2: Resistive Switching Test Circuit & Waveform

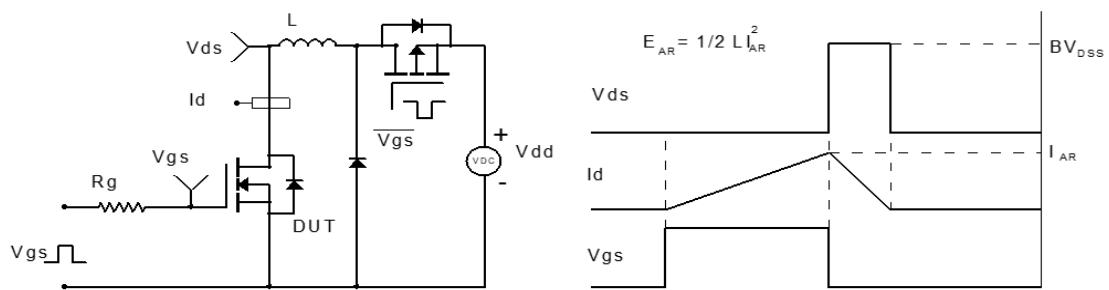


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

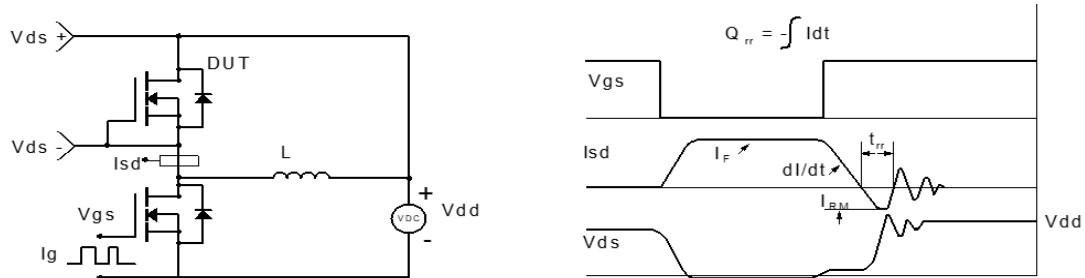
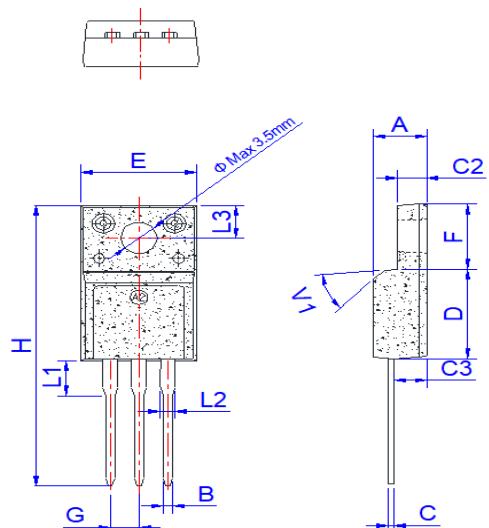


Figure 4: Diode Recovery Test Circuit & Waveform



Package Mechanical Data(TO-220FP-3L)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.50		4.90	0.177		0.193
B	0.74	0.80	0.83	0.029	0.031	0.033
C	0.47		0.65	0.019		0.026
C2	2.45		2.75	0.096		0.108
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.80		10.4	0.386		0.410
F	6.40		6.80	0.252		0.268
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.63			0.143	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	

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