

Description

JMT P-channel Enhancement Mode Power MosFET

Features

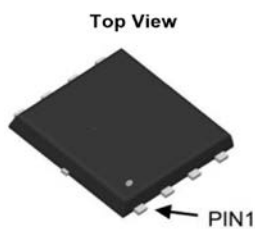
- -30V, -50A
- $R_{DS(ON)} < 7m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} < 10m\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

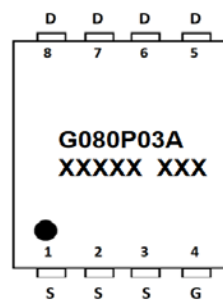
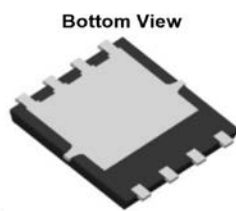
- Load Switch
- PWM Application
- Power Management



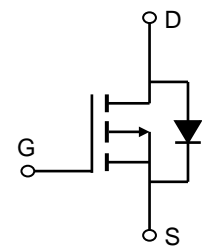
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN5x6-8L



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
G080P03A	JMTG080P03A	TAPING	PDFN5x6-8L	13"	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	-50
		$T_C = 100^\circ C$	-32
I_{DM}	Pulsed Drain Current ⁽¹⁾	-200	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	132	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	57
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	36	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.2	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.8	-2.5	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = -10V, I _D = -20A	-	5.4	7	mΩ
		V _{GS} = -4.5V, I _D = -10A	-	7.6	10	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	-	3366	-	pF
C _{oss}	Output Capacitance		-	471	-	pF
C _{rss}	Reverse Transfer Capacitance		-	324	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -10V V _{DS} = -15V, I _D = -10A	-	59	-	nC
Q _{gs}	Gate Source Charge		-	10	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	14	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = -10V, V _{DD} = -15V I _D = -10A, R _{GEN} = 3Ω	-	7	-	ns
t _r	Turn-On Rise Time		-	6	-	ns
t _{d(off)}	Turn-Off DelayTime		-	112	-	ns
t _f	Turn-Off Fall Time		-	78	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-50	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-200	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -30A	-	-	-1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = -10A, di/dt = 100A/us	-	21	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	10	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting T_J=25C, V_{DD}=-15V, V_G=-10V, R_G=25ohm, L=0.5mH, I_{AS}=-23A
 3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

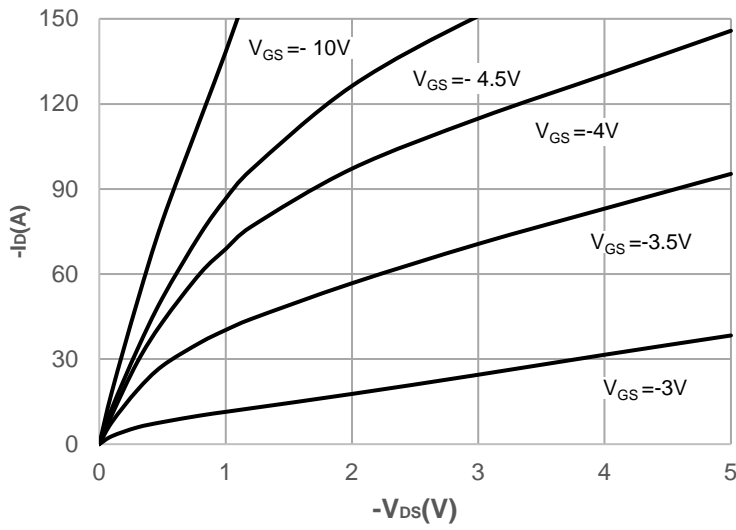


Figure 2: Typical Transfer Characteristics

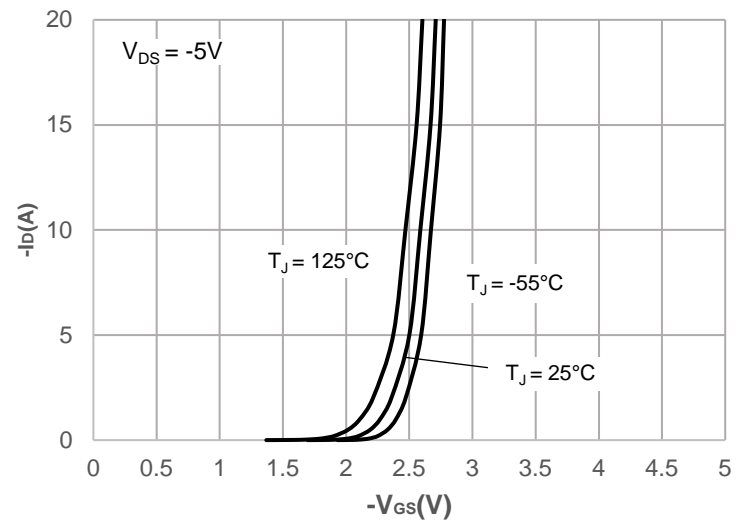


Figure 3: On-resistance vs. Drain Current

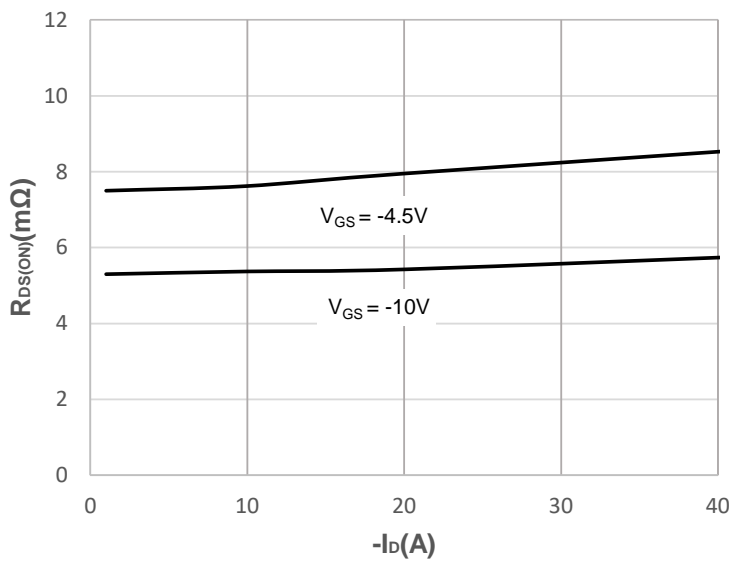


Figure 4: Body Diode Characteristics

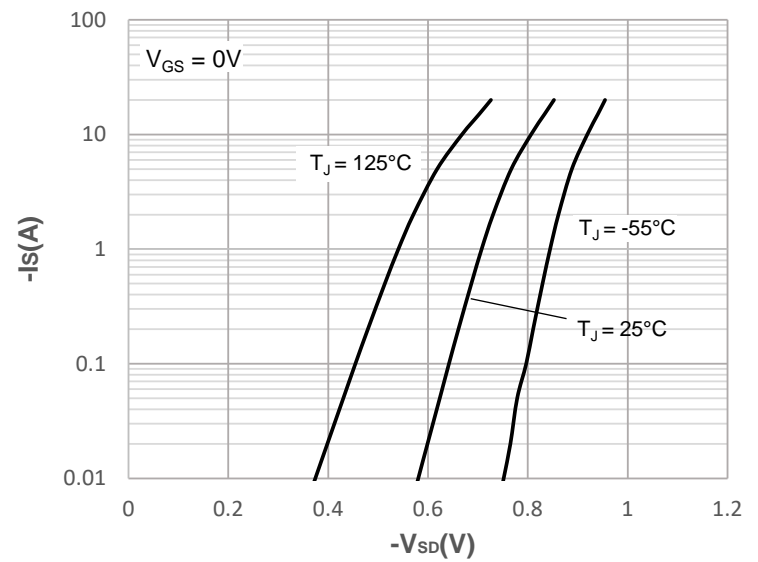


Figure 5: Gate Charge Characteristics

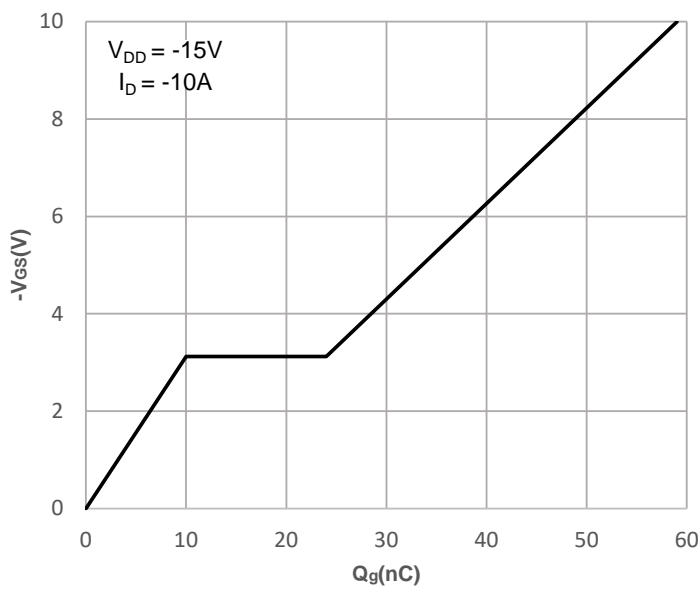
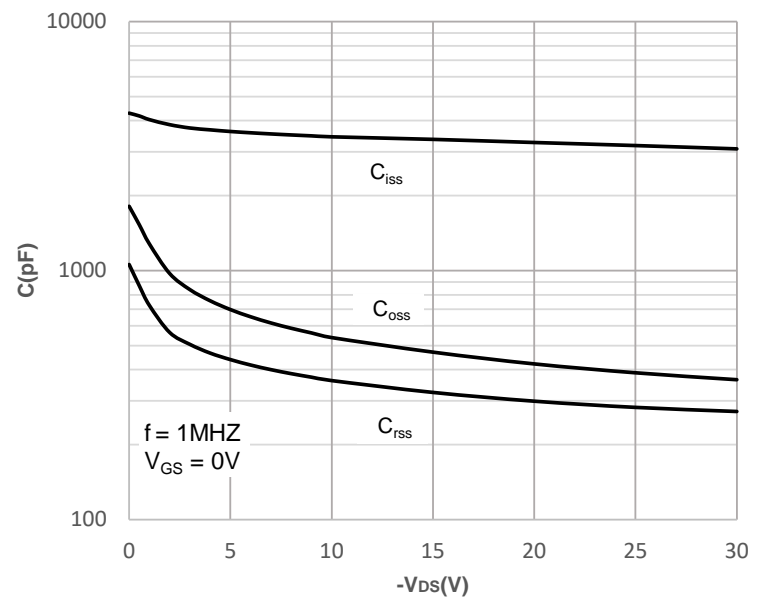


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

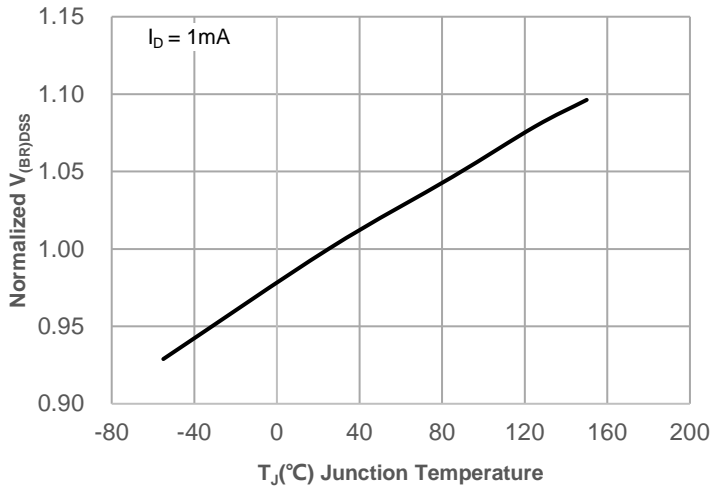


Figure 8: Normalized on Resistance vs. Junction Temperature

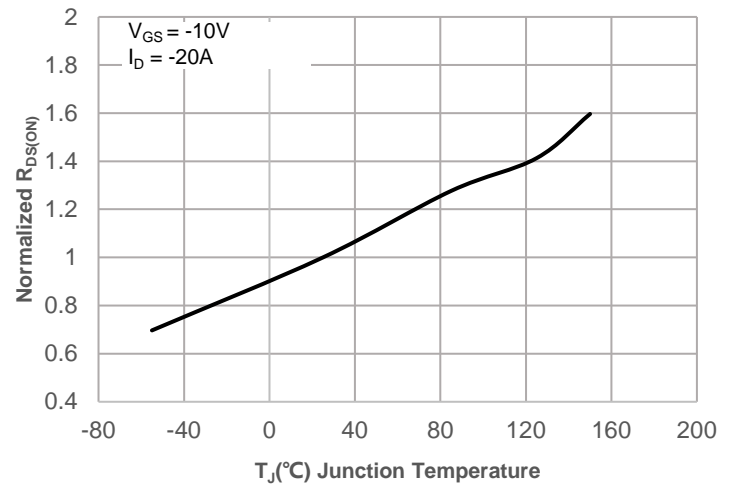


Figure 9: Maximum Safe Operating Area

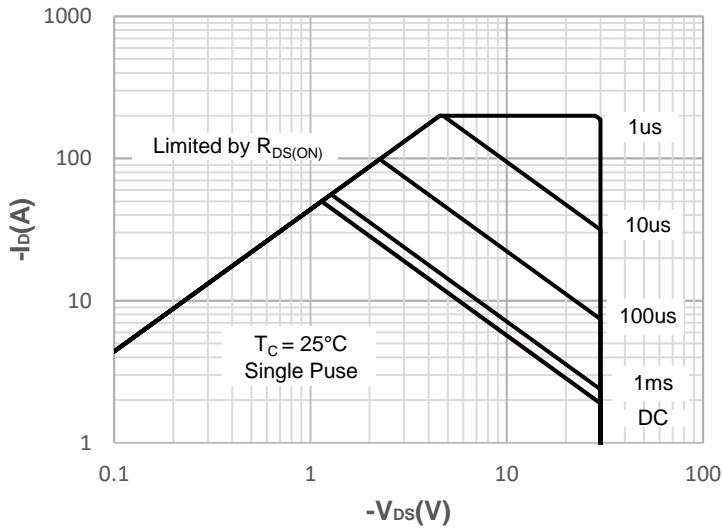


Figure 10: Maximum Continuous Driant Current vs. Case Temperature

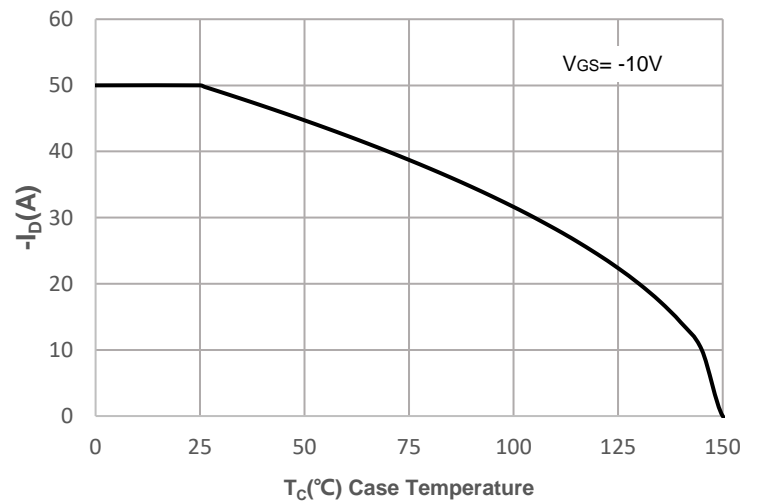


Figure 11: Normalized Maximum Transient Thermal Impedance

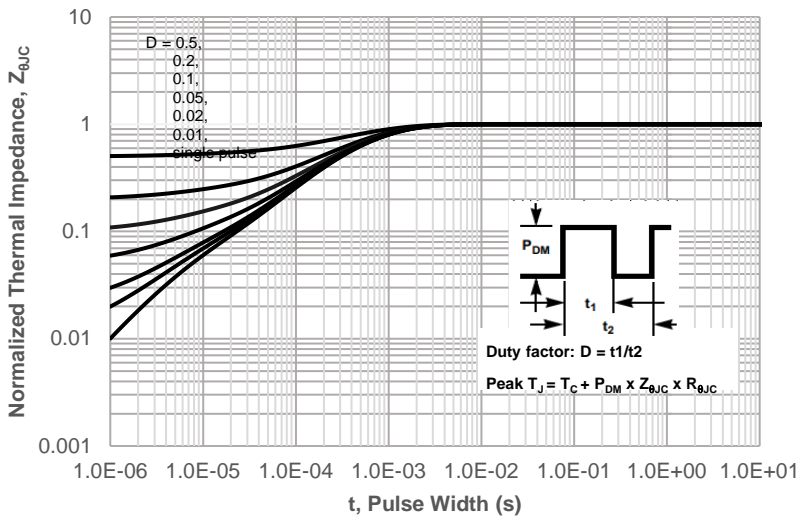
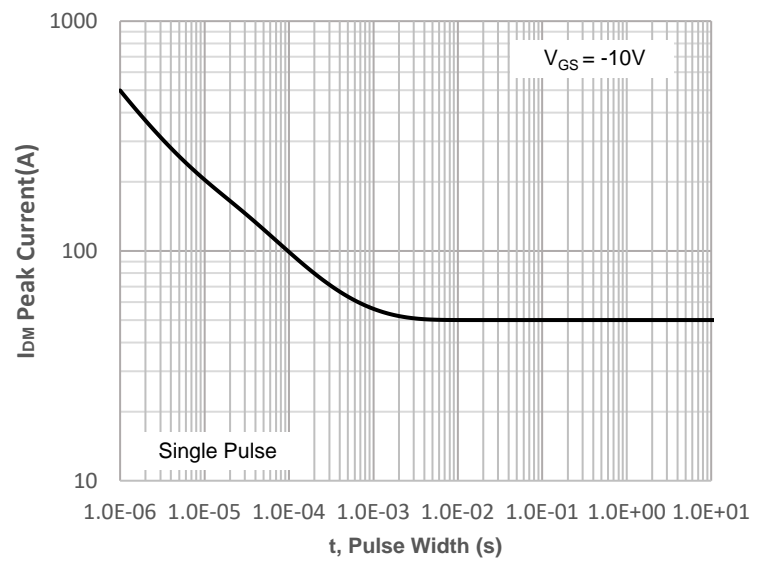


Figure 12: Peak Current Capacity



Test Circuit

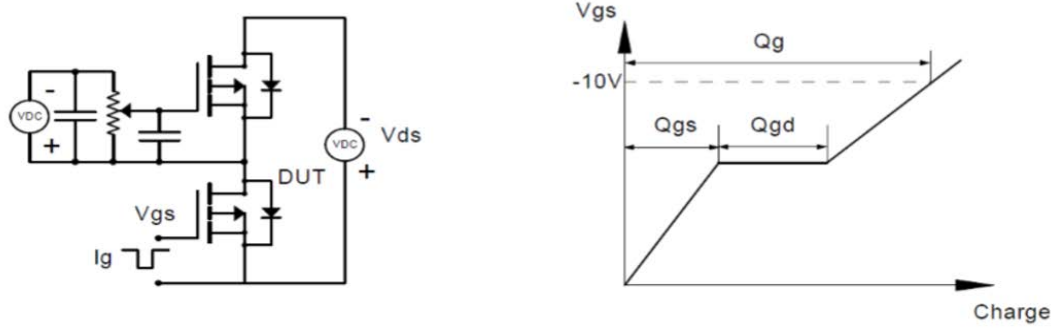


Figure 1: Gate Charge Test Circuit & Waveform

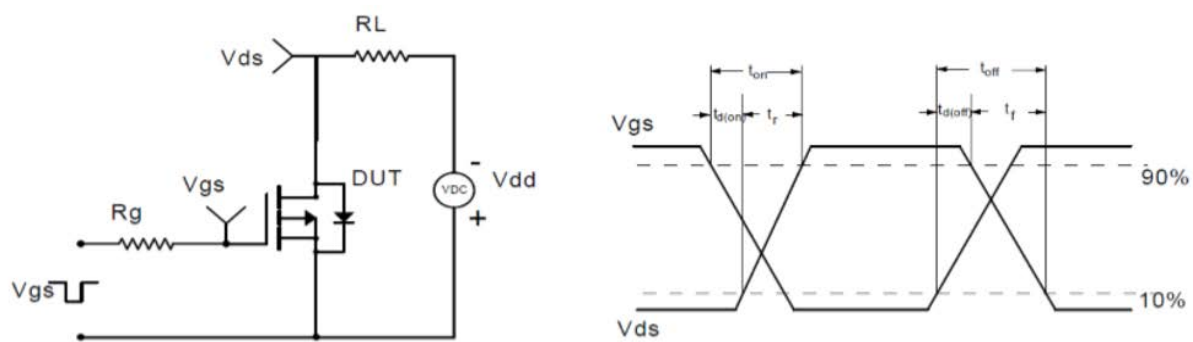


Figure 2: Resistive Switching Test Circuit & Waveform

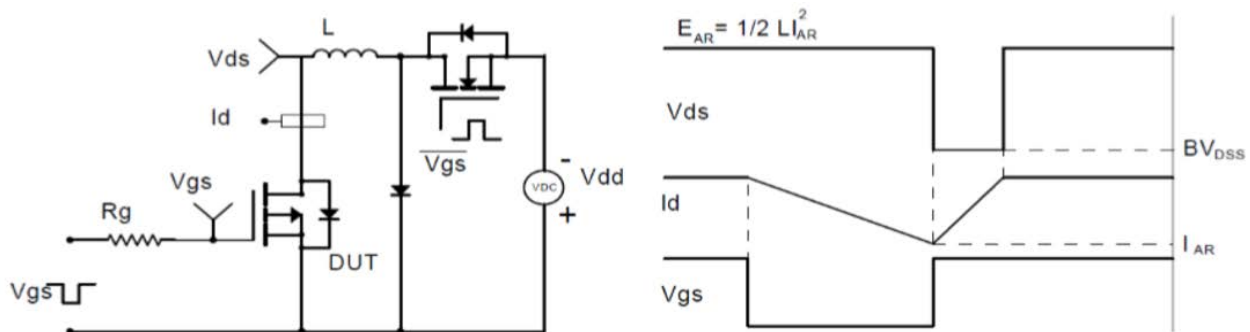


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

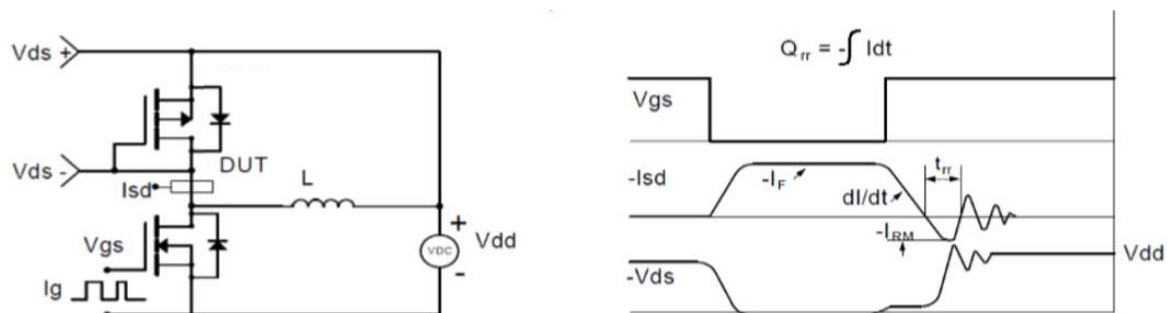
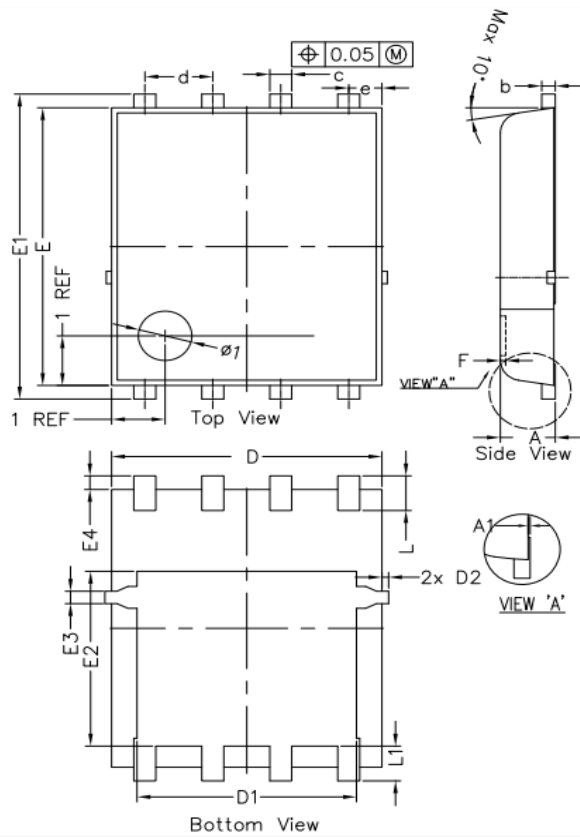


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN5x6-8L)



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
* A	0.900	1.000	1.100	0.035	0.039	0.043
A1	0.000	---	0.050	0.000	----	0.002
b	0.246	0.254	0.312	0.010	0.010	0.012
* c	0.310	0.410	0.510	0.012	0.016	0.020
d	1.27 BSC			0.050 BSC		
* D	4.950	5.050	5.150	0.195	0.199	0.203
D1	4.000	4.100	4.200	0.157	0.161	0.165
* D2	---	---	0.125	---	---	0.005
e	0.62 BSC			0.024 BSC		
* E	5.500	5.600	5.700	0.217	0.220	0.224
* E1	6.050	6.150	6.250	0.238	0.242	0.246
E2	3.425	3.525	3.625	0.135	0.139	0.143
E3	0.150	0.250	0.350	0.006	0.010	0.014
* E4	0.175	0.275	0.375	0.007	0.011	0.015
F	-	-	0.100	-	-	0.004
* L	0.500	0.600	0.700	0.02	0.02	0.03
L1	0.600	0.700	0.800	0.02	0.03	0.03

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