



Description

JMT P-channel Enhancement Mode Power MOSFET

Features

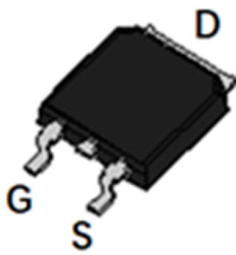
- $V_{DS} = -40V$, $I_D = -70A$
 $R_{DS(ON)} < 9.2m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 13m\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

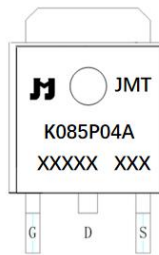
- PWM Applications
- Load Switch
- Power Management



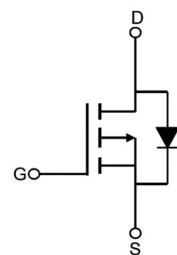
100% UIS TESTED!
100% ΔVds TESTED!



TO-252-3L(DPAK) top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMTK085P04A	JMTK085P04A	TAPING	TO-252-3L	13inch	2500	25000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	-70
		$T_C = 100^\circ C$	-46
I_{DM}	Pulsed Drain Current ^{note1}	-280	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	182	mJ
P_D	Power Dissipation	90	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.5	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} = -10V, I _D = -30A	-	7.1	9.2	mΩ
		V _{GS} = -4.5V, I _D = -20A	-	9.3	13	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} =0V, f=1.0MHz	-	7200	-	pF
C _{oss}	Output Capacitance		-	625	-	pF
C _{rss}	Reverse Transfer Capacitance		-	437	-	pF
Q _g	Total Gate Charge	V _{DS} = -20V, I _D = -20A, V _{GS} = -10V	-	115	-	nC
Q _{gs}	Gate-Source Charge		-	23	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	20	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -20V, I _D = -20A, V _{GS} = -10V, R _{GEN} =3Ω	-	15	-	ns
t _r	Turn-on Rise Time		-	88	-	ns
t _{d(off)}	Turn-off Delay Time		-	122	-	ns
t _f	Turn-off Fall Time		-	101	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-70	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-280	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -30A	-	-	-1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S = -20A, di/dt=100A/μs	-	25	-	ns
Q _{rr}	Reverse Recovery Charge		-	17	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J= 25°C, V_{DD}= -20V, V_G= -10V, L= 0.5mH, R_G= 25Ω, I_{AS}= -27A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%



Typical Performance Characteristics

Figure 1: Output Characteristics

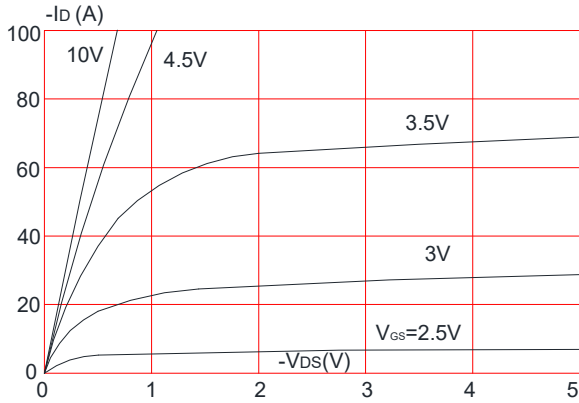


Figure 2: Typical Transfer Characteristics

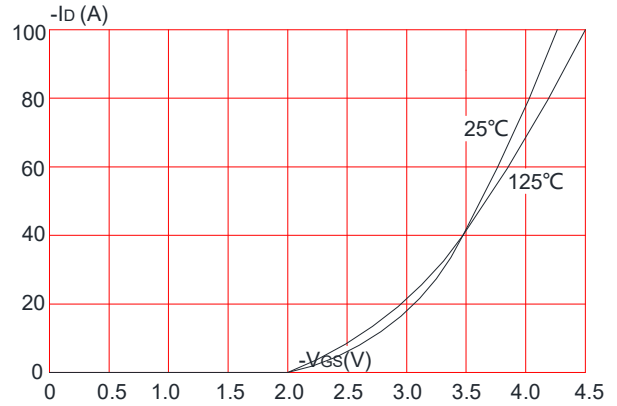


Figure 3: On-resistance vs. Drain Current

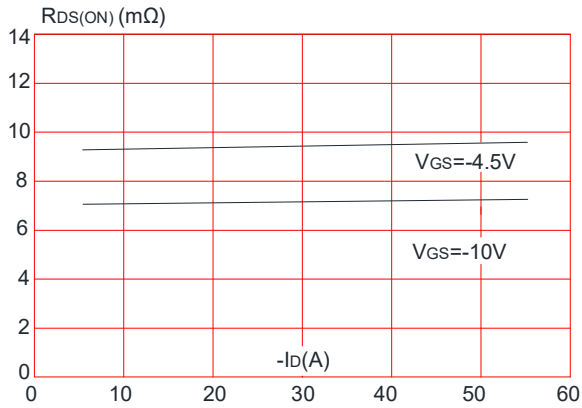


Figure 4: Body Diode Characteristics

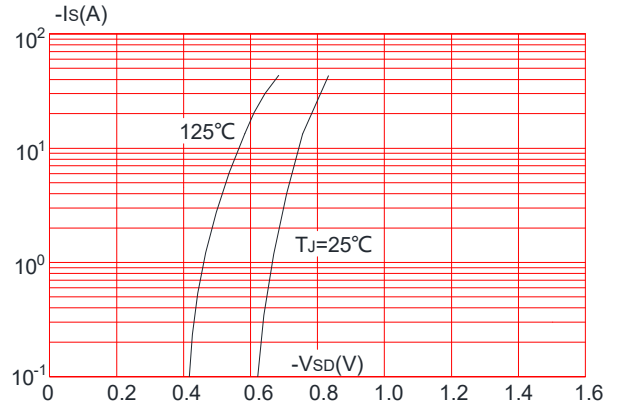


Figure 5: Gate Charge Characteristics

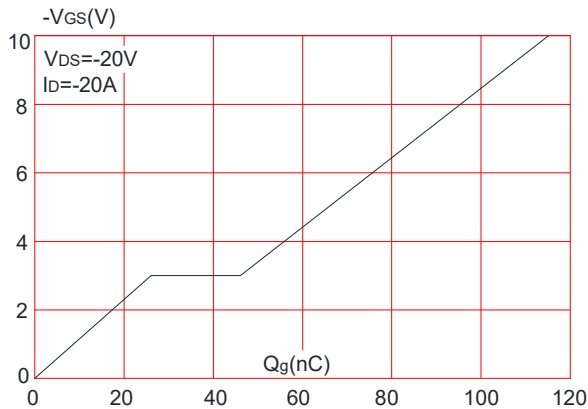


Figure 6: Capacitance Characteristics

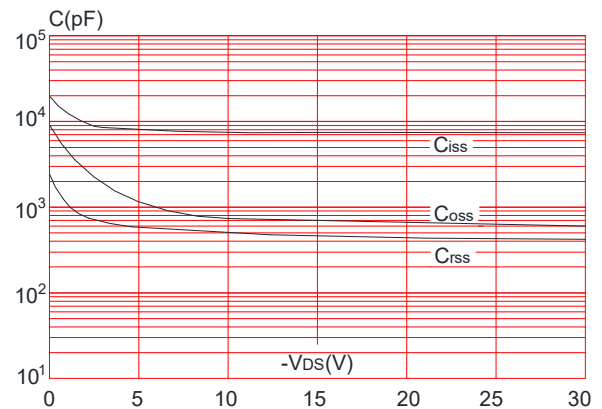




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

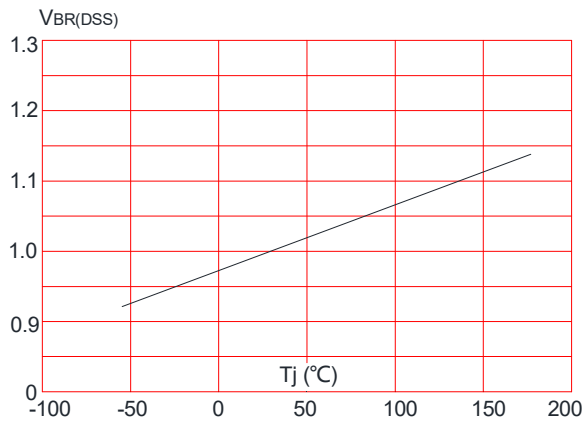


Figure 8: Normalized on Resistance vs. Junction Temperature

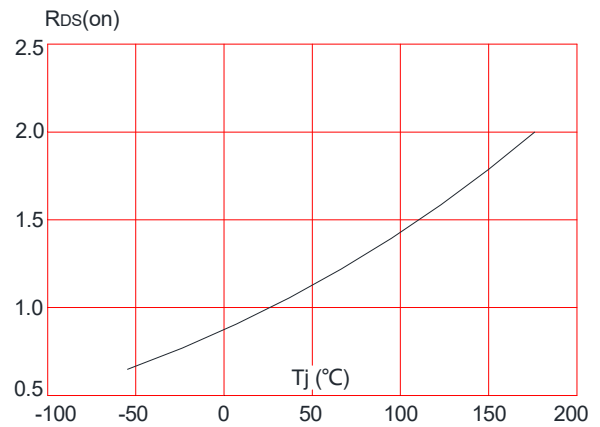


Figure 9: Maximum Safe Operating Area

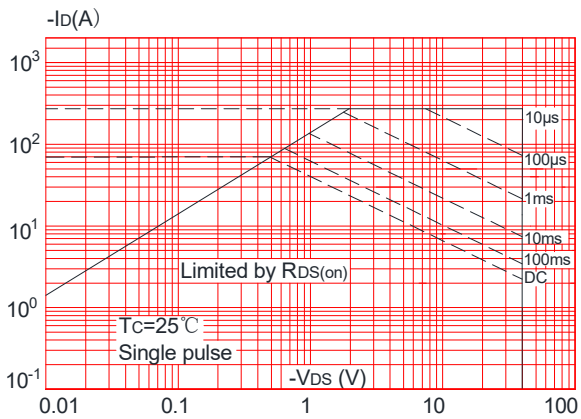


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

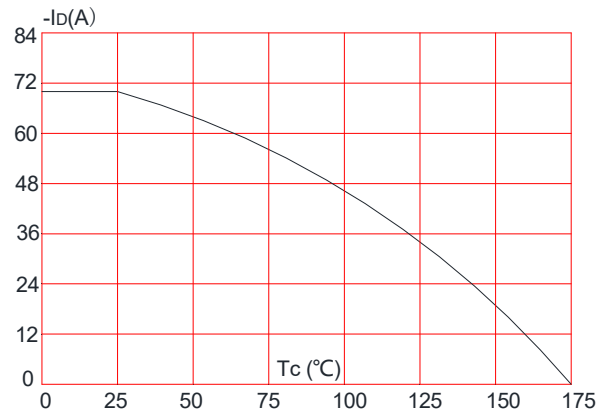
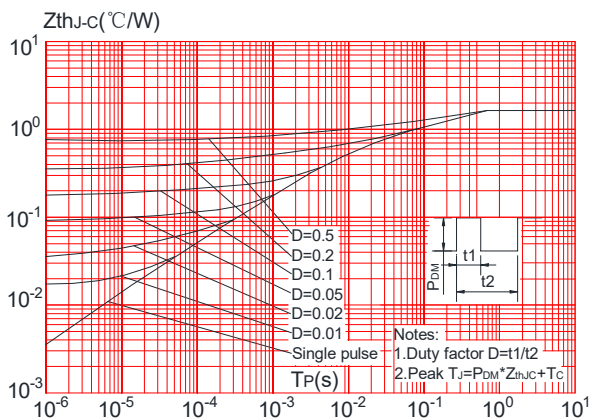
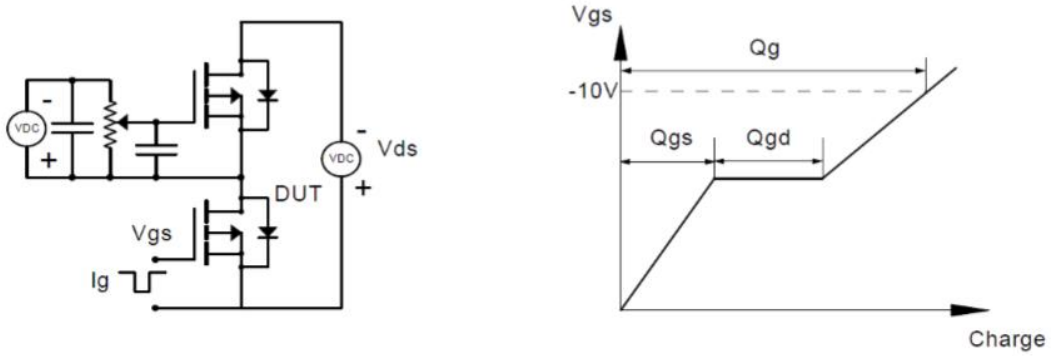


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

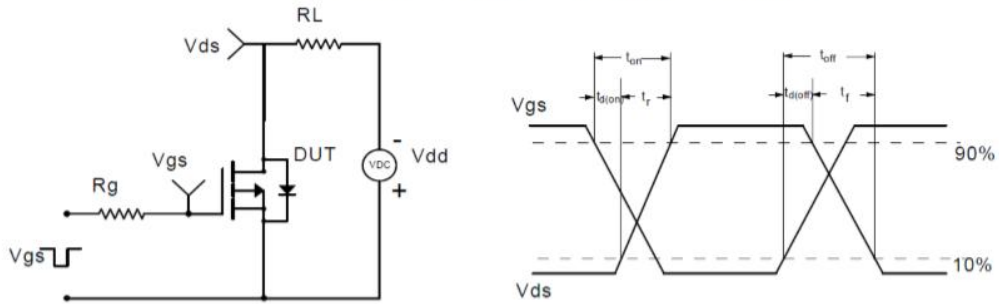


Test Circuit

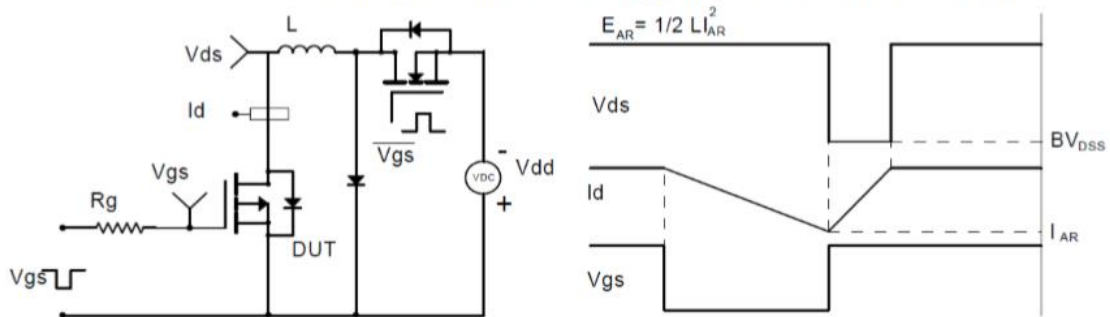
Gate Charge Test Circuit & Waveform



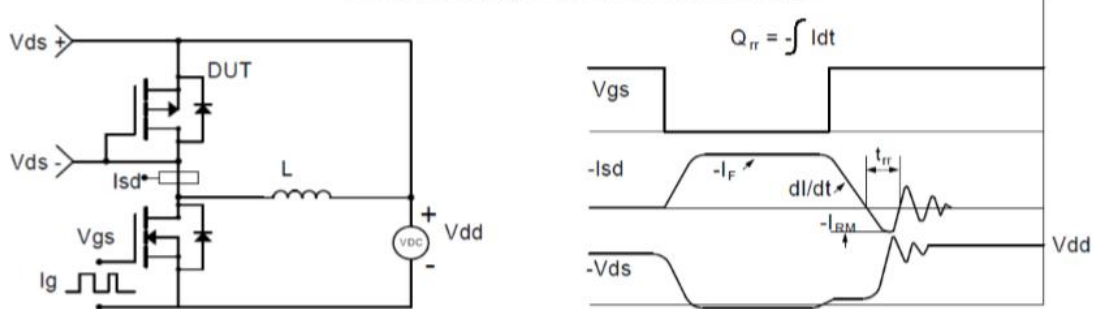
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

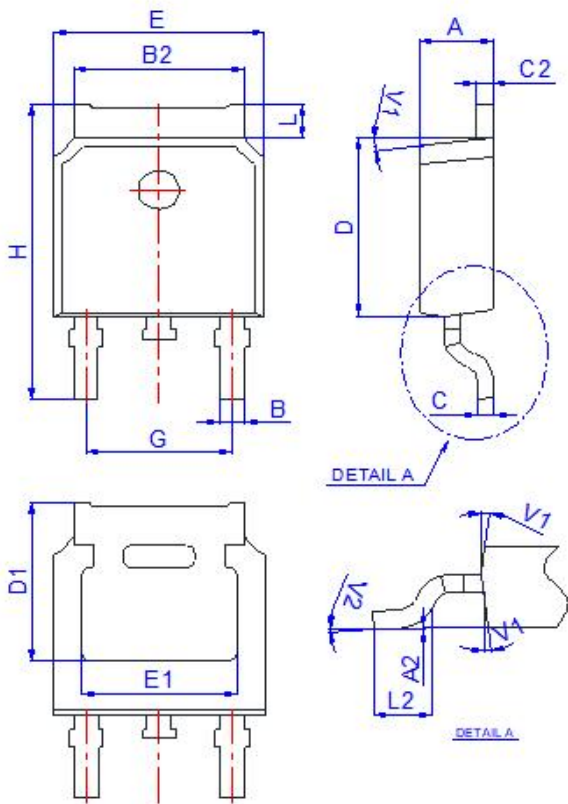


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data-TO-252-3L




Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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