

## Description

### JMT N-channel Enhancement Mode Power MOSFET

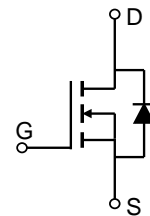
#### Features

- z 20V, 60A
- z  $R_{DS(ON)} < 6.2m \quad \# V_{GS} = 4.5V$
- z  $R_{DS(ON)} < 8.5m \quad \# V_{GS} = 2.5V$
- z Advanced Trench Technology
- z Excellent  $R_{DS(ON)}$  and Low Gate Charge
- z Lead Free

#### Applications

- z Load Switch
- z PWM Application
- z Power Management

100% UIS TESTED!  
100%  $\dot{U}_{Vds}$  TESTED!



TO-252-3L(DPAK) Top View

Marking and Pin Assignment

Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
JMTK2006A	JMTK2006A	TAPING	TO-252-3L	13"	2500	25000

## Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	60
		$T_C = 100^\circ C$	38
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	240	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(2)</sup>	64	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ C$	37
$R_{\theta SA}$	Thermal Resistance, Junction to Ambient <sup>(3)</sup>	32	$^\circ C/W$
$R_{\theta SC}$	Thermal Resistance, Junction to Case	3.4	
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	$^\circ C$



## Typical Performance Characteristics

Figure 1: Output Characteristics

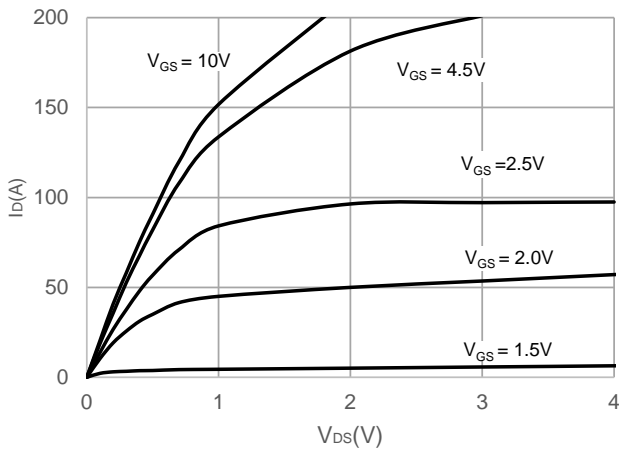


Figure 2: Typical Transfer Characteristics

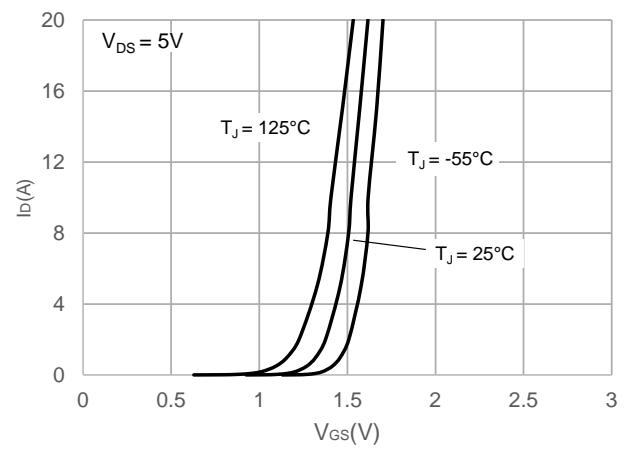


Figure 3: On- resistance vs. Drain Current

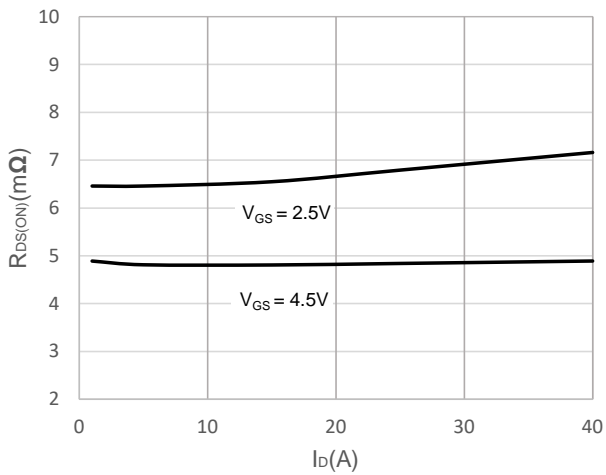


Figure 4: Body Diode Characteristics

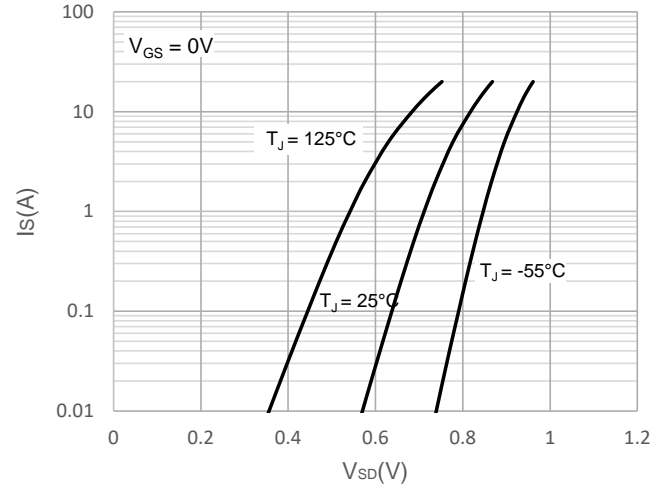


Figure 5: Gate Charge Characteristics

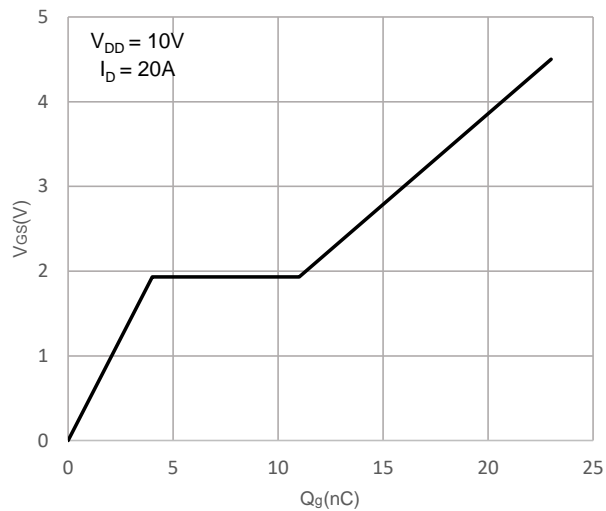
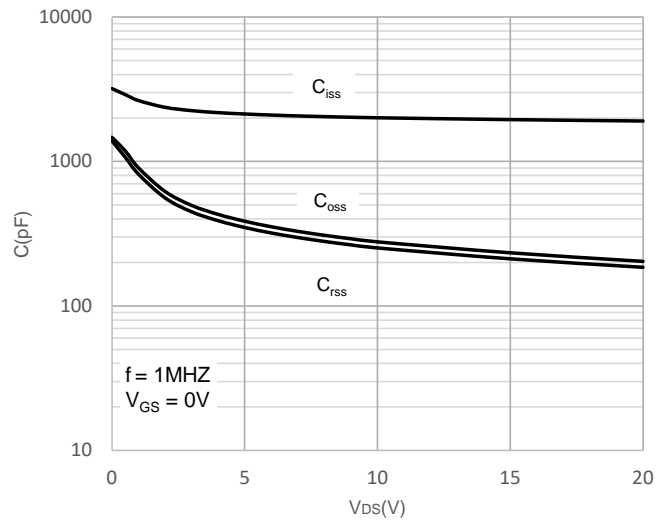


Figure 6: Capacitance Characteristics



## Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

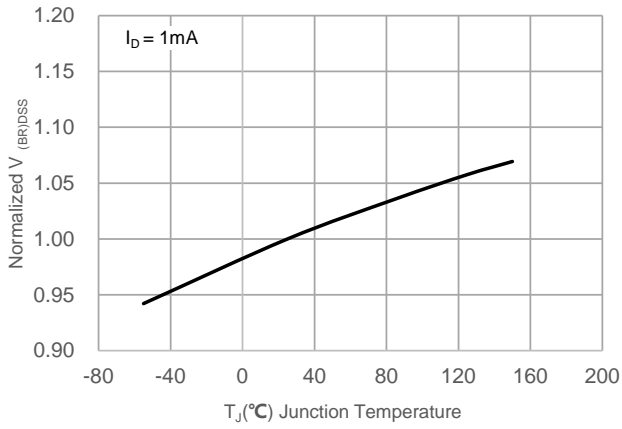


Figure 8: Normalized on Resistance vs. Junction Temperature

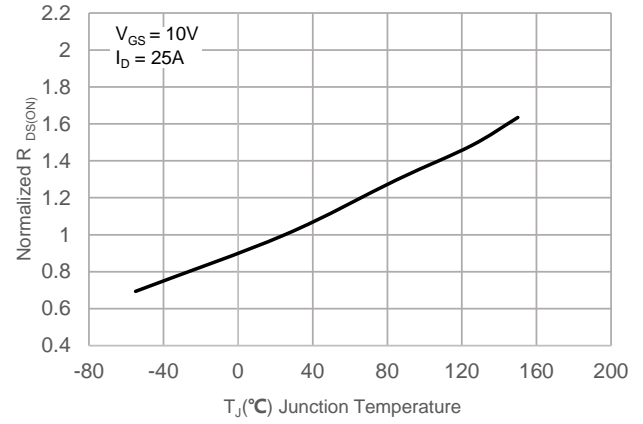


Figure 9: Maximum Safe Operating Area

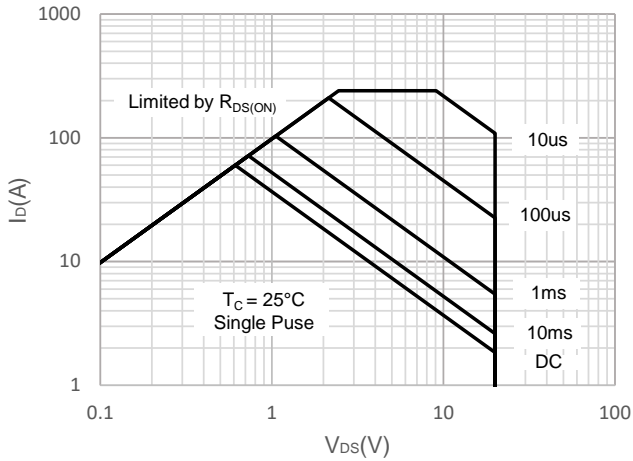


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

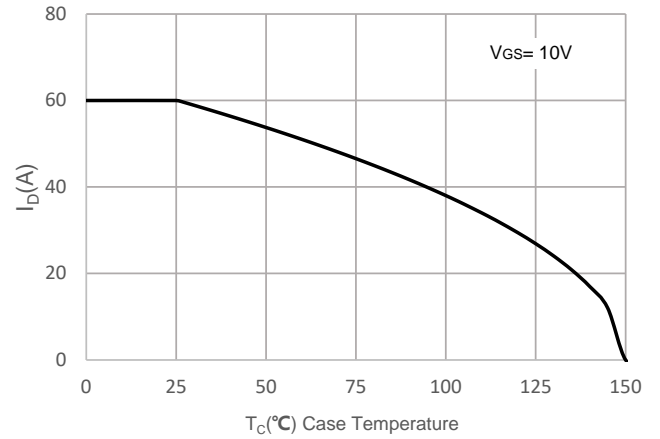


Figure 11: Normalized Maximum Transient Thermal Impedance

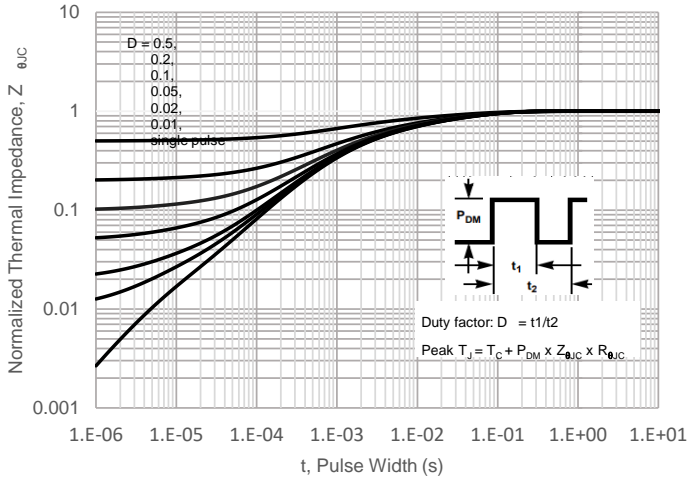
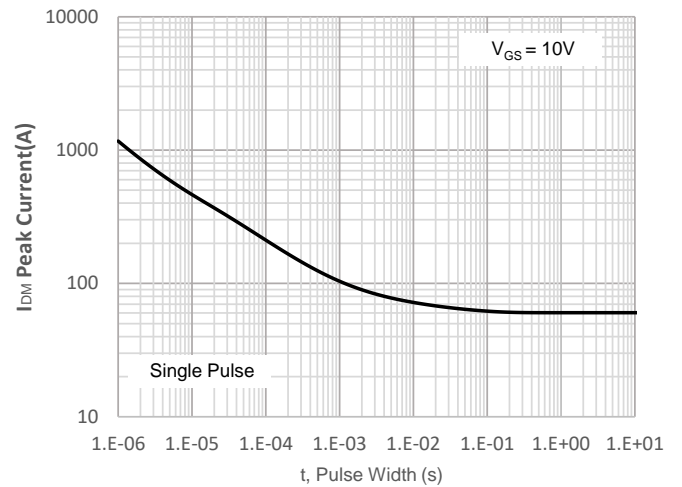


Figure 12: Peak Current Capacity



## Test Circuit

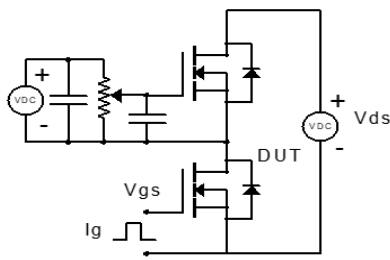


Figure 1: Gate Charge Test Circuit & Waveform

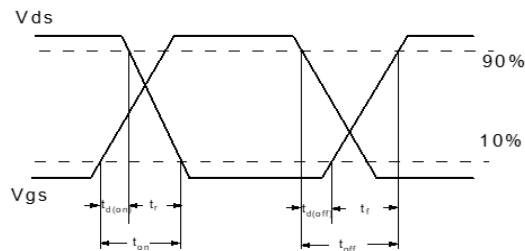


Figure 2: Resistive Switching Test Circuit & Waveform

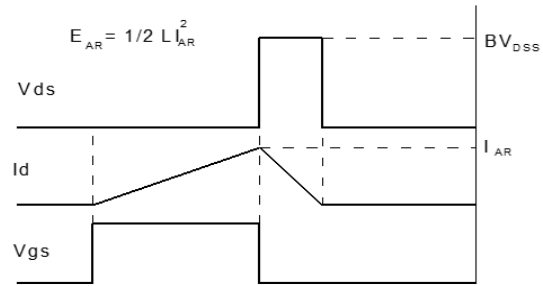
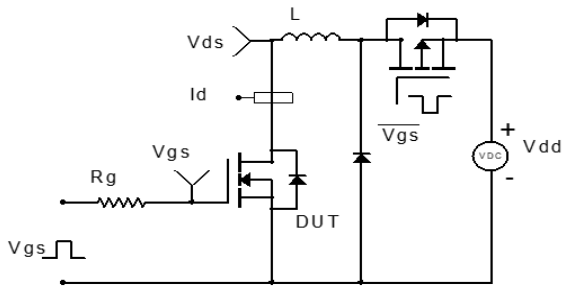


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

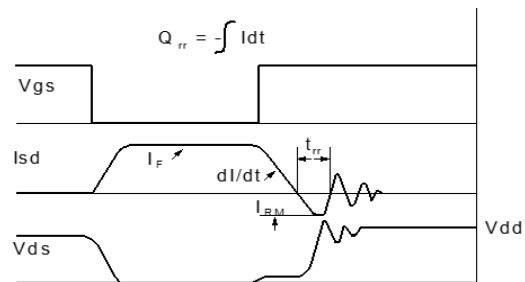
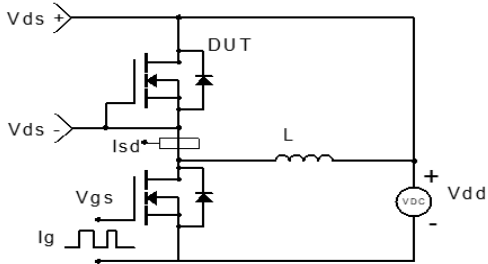
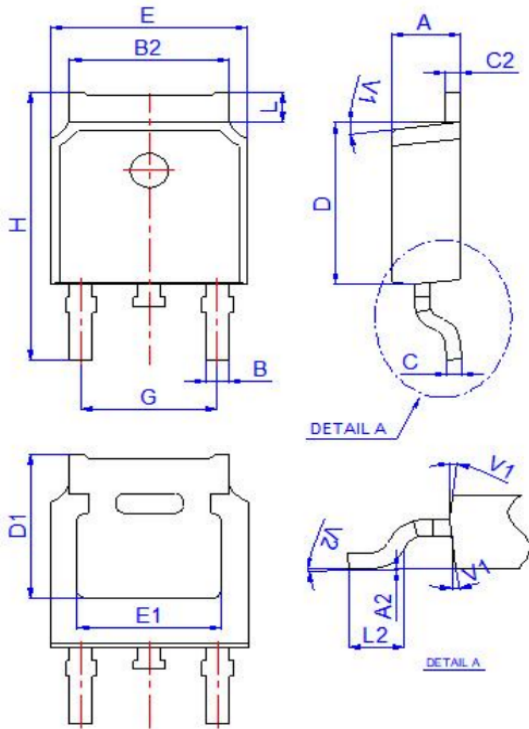



Figure 4: Diode Recovery Test Circuit & Waveform

## Package Mechanical Data(TO-252-3L)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

 is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.  
 Copyright ©2023 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.