

## Description

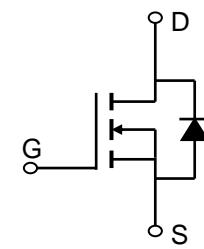
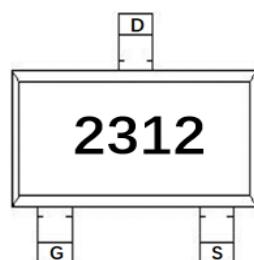
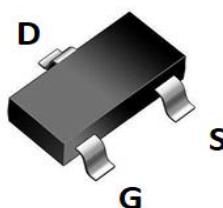
### JMT N-channel Enhancement Mode Power MOSFET

#### Features

- 20V, 6.8A
- $R_{DS(ON)} < 21\text{m}\Omega$  @  $V_{GS} = 4.5\text{V}$
- $R_{DS(ON)} < 25\text{m}\Omega$  @  $V_{GS} = 2.5\text{V}$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free

#### Applications

- Load Switch
- PWM Application
- Power Management



SOT-23 Top View

Marking and Pin Assignment

Schematic Diagram

#### Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
2312	JMTL2312A	TAPING	SOT-23	7"	3000	120000

#### Absolute Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Value	Units
$V_{DS}$	Drain-to-Source Voltage		20	V
$V_{GS}$	Gate-to-Source Voltage		$\pm 12$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ\text{C}$	6.8	A
		$T_A = 100^\circ\text{C}$	4	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>		27	A
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$	1.3	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(2)</sup>		97	$^\circ\text{C}/\text{W}$
$T_J, T_{STG}$	Junction & Storage Temperature Range		-55 to 150	$^\circ\text{C}$

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

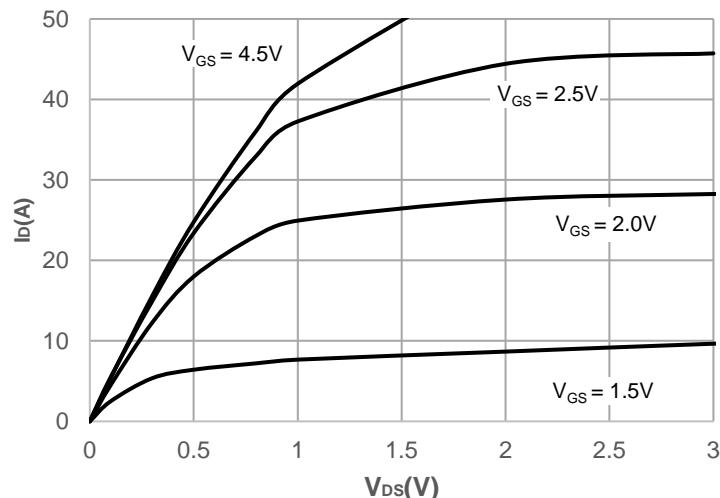
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.5	0.75	1.0	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 4.5\text{V}, I_D = 4\text{A}$	-	16	21	$\text{m}\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 3\text{A}$	-	19	25	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 10\text{V}, f = 1\text{MHz}$	-	712	-	pF
$C_{\text{oss}}$	Output Capacitance		-	116	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	103	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 4.5\text{V}$ $V_{DD} = 10\text{V}, I_D = 3\text{A}$	-	9	-	nC
$Q_{gs}$	Gate Source Charge		-	1.5	-	nC
$Q_{gd}$	Gate Drain("Miller") Charge		-	2.5	-	nC
<b>Switching Characteristics</b>						
$t_{d(\text{on})}$	Turn-On DelayTime	$V_{GS} = 4.5\text{V}, V_{DD} = 10\text{V}$ $I_D = 3\text{A}, R_{\text{GEN}} = 3\Omega$	-	5	-	ns
$t_r$	Turn-On Rise Time		-	16	-	ns
$t_{d(\text{off})}$	Turn-Off DelayTime		-	23	-	ns
$t_f$	Turn-Off Fall Time		-	7	-	ns
<b>Drain-Source Diode Characteristics and Max Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	6.8	A	
$I_{\text{SM}}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	27	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 6.8\text{A}$	-	-	1.2	V
$trr$	Body Diode Reverse Recovery Time	$I_F = 3\text{A}, di/dt = 100\text{A/us}$	-	7	-	ns
$Qrr$	Body Diode Reverse Recovery Charge		-	2	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

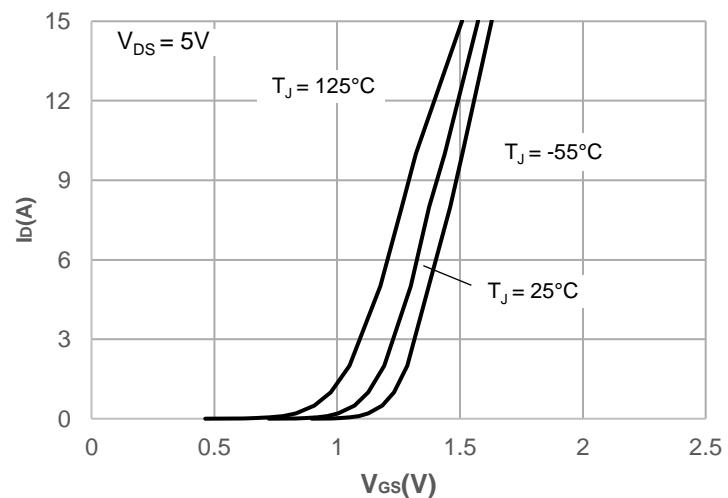
2.  $R_{\theta JA}$  is measured with the device mounted on a 1inch<sup>2</sup> pad of 2oz copper FR4 PCB3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .

## Typical Performance Characteristics

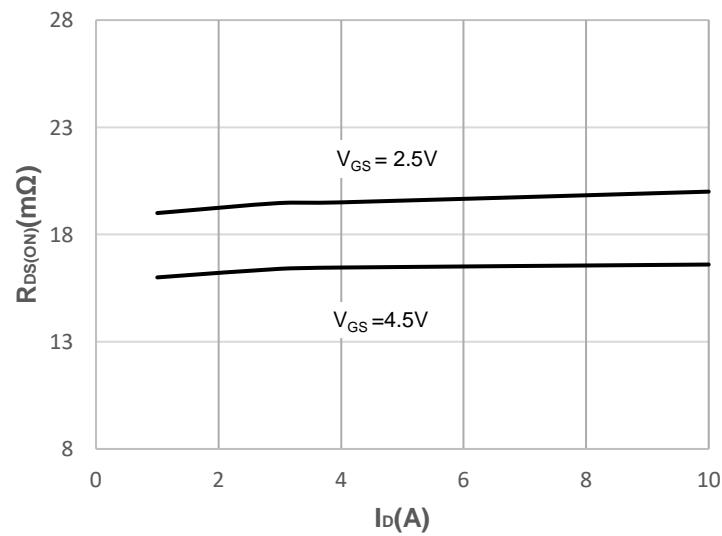
**Figure 1: Output Characteristics**



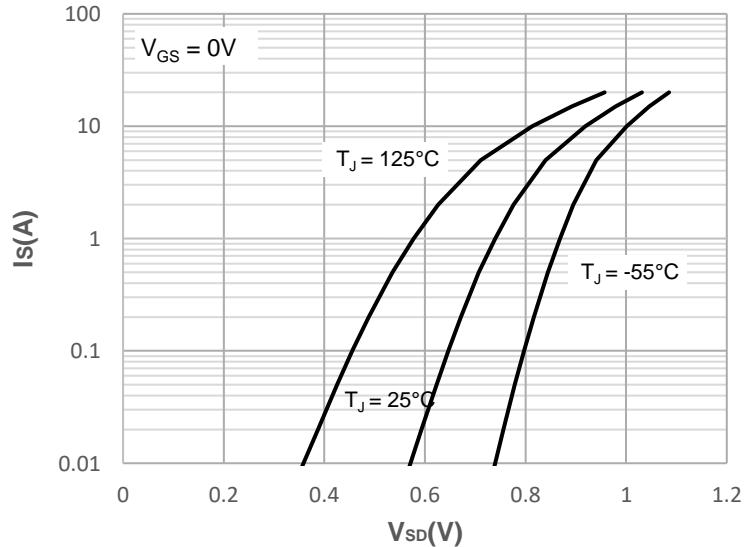
**Figure 2: Typical Transfer Characteristics**



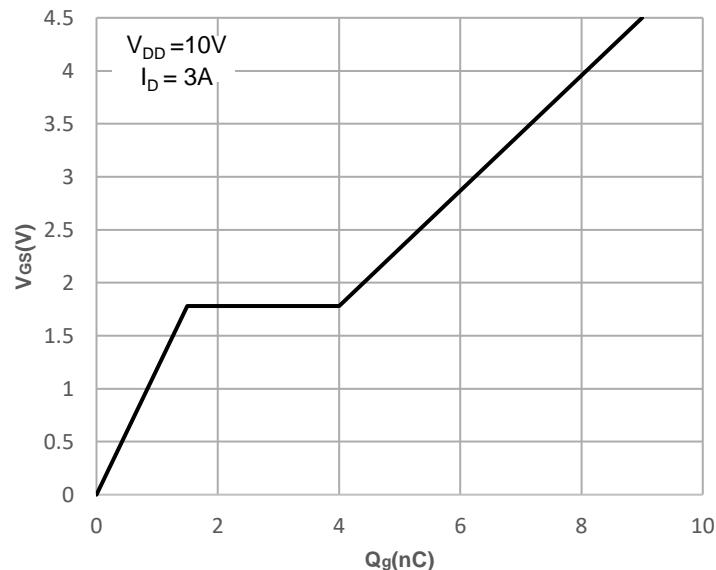
**Figure 3: On-resistance vs. Drain Current**



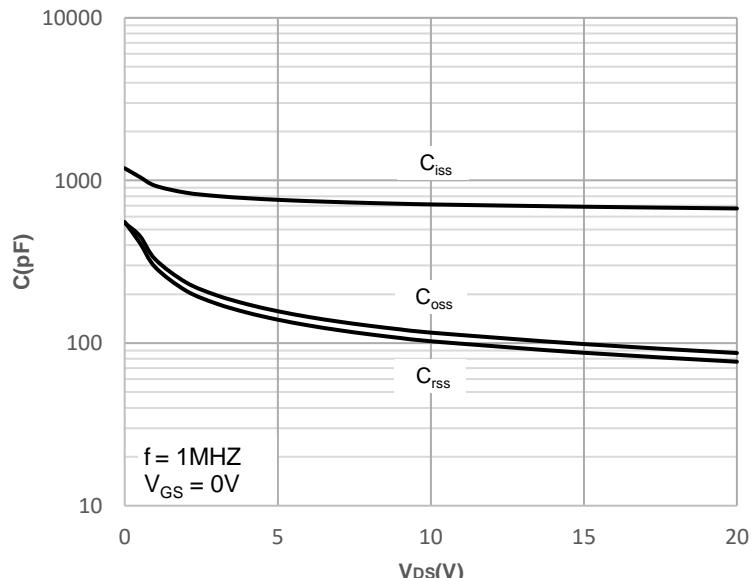
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**

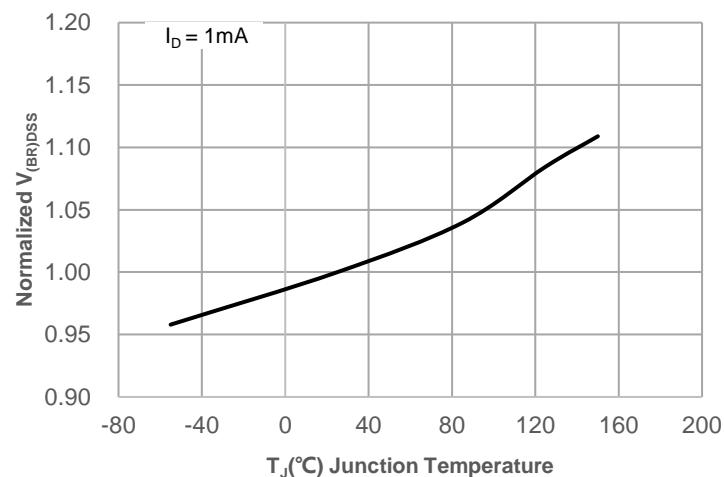


**Figure 6: Capacitance Characteristics**

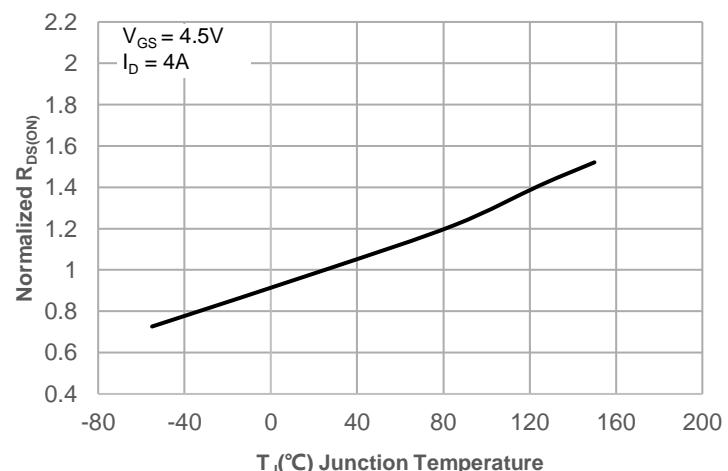


## Typical Performance Characteristics

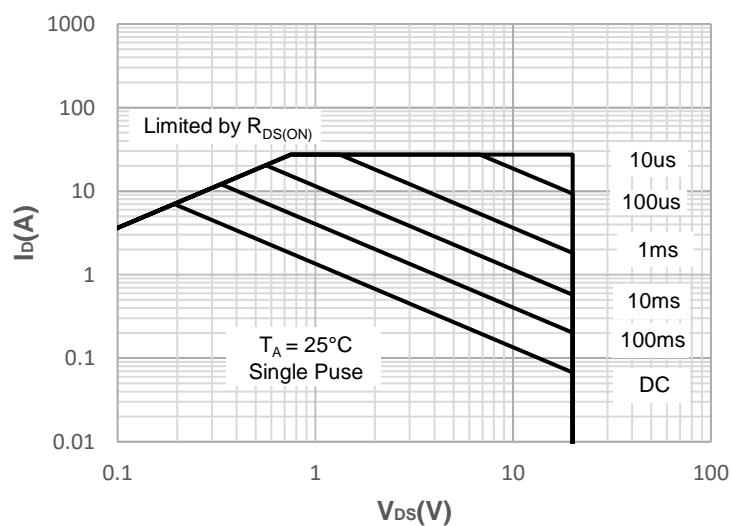
**Figure 7: Normalized Breakdown voltage vs. Junction Temperature**



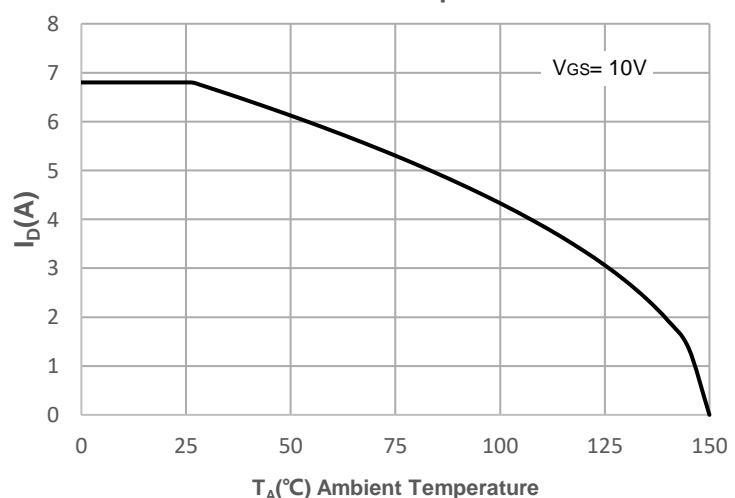
**Figure 8: Normalized on Resistance vs. Junction Temperature**



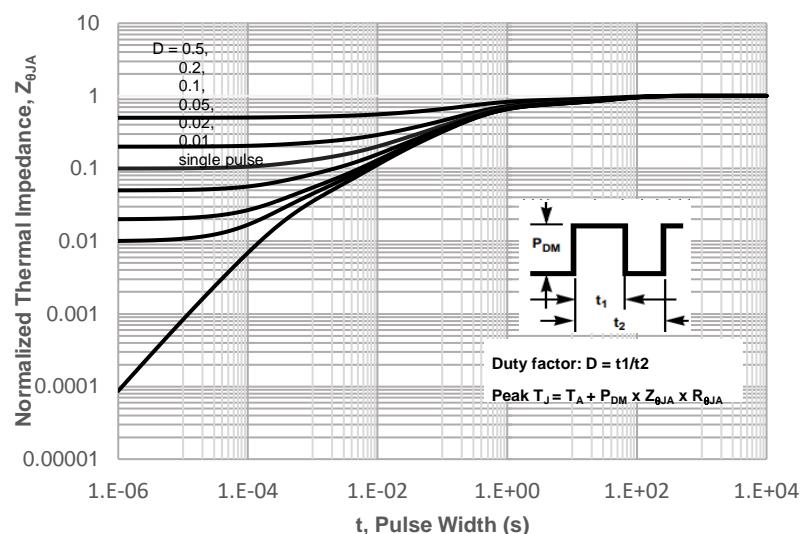
**Figure 9: Maximum Safe Operating Area**



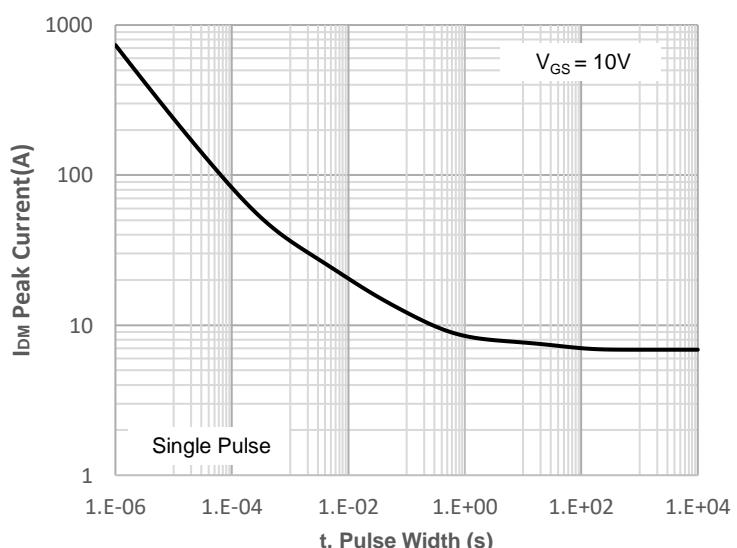
**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



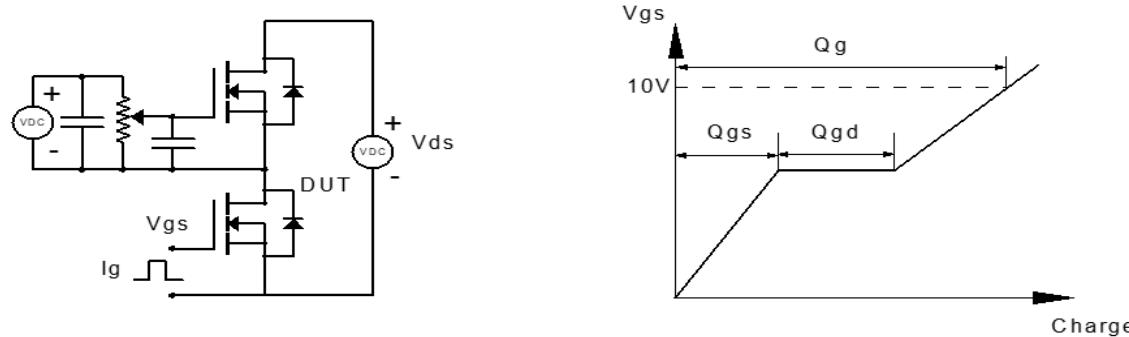
**Figure 11: Normalized Maximum Transient Thermal Impedance**



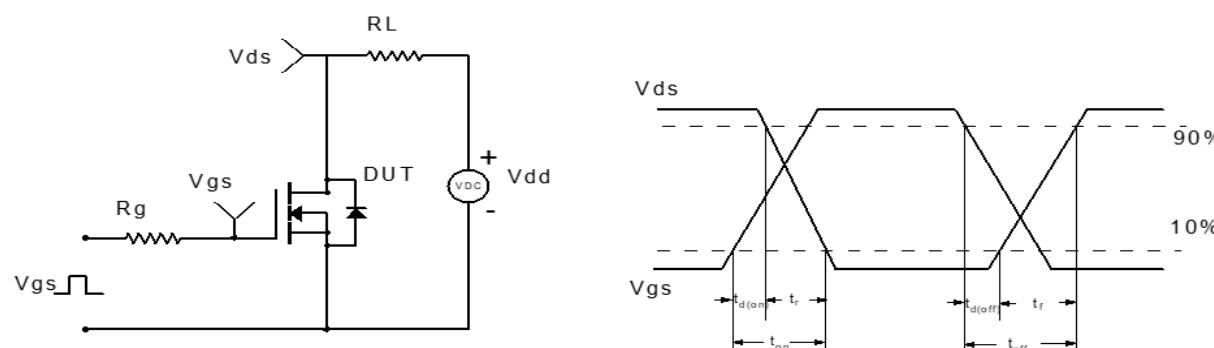
**Figure 12: Peak Current Capacity**



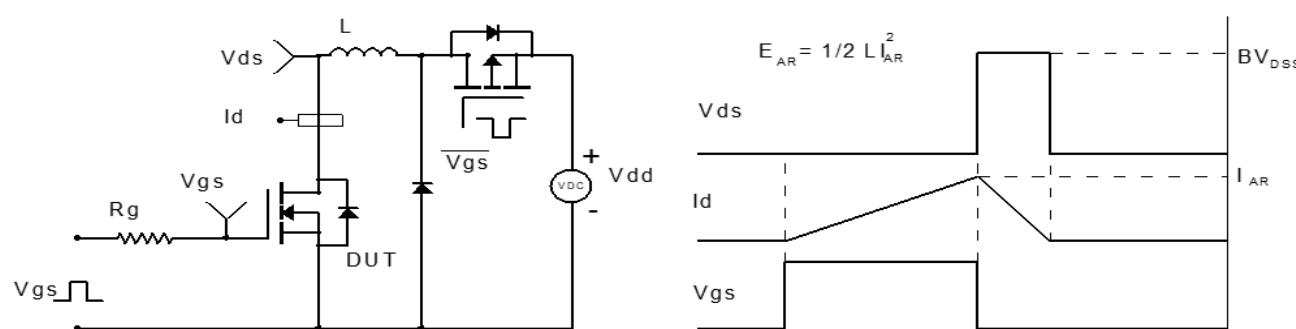
## Test Circuit



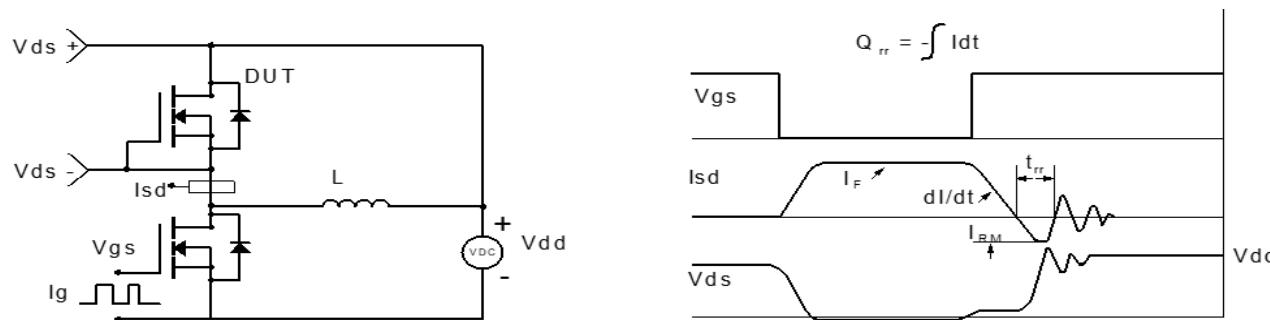
**Figure 1: Gate Charge Test Circuit & Waveform**



**Figure 2: Resistive Switching Test Circuit & Waveform**

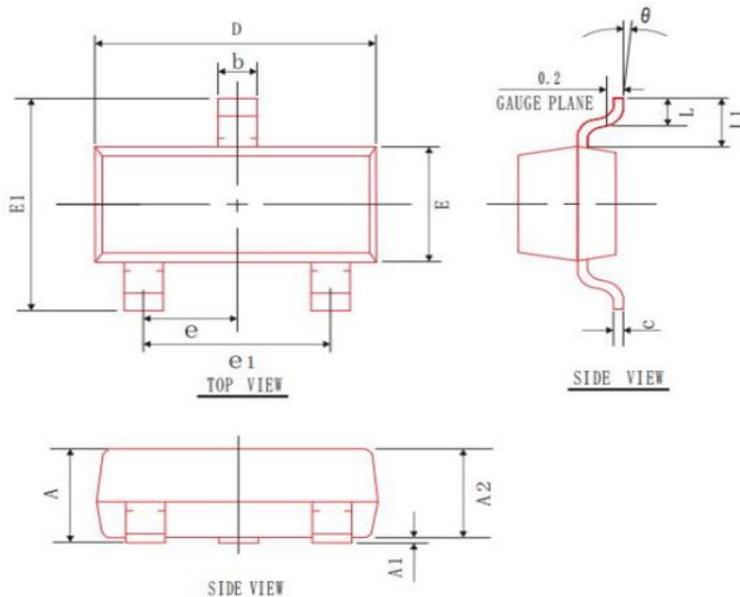


**Figure 3: Unclamped Inductive Switching Test Circuit & Waveform**



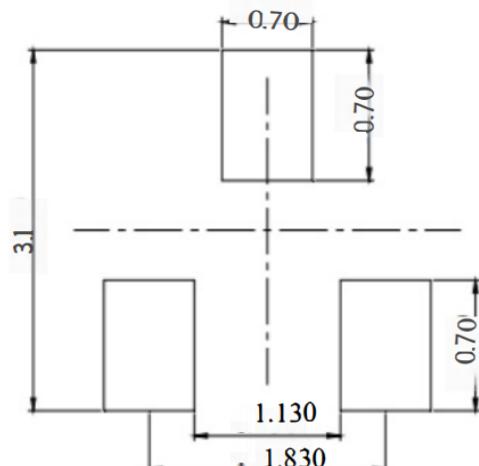
**Figure 4: Diode Recovery Test Circuit & Waveform**

## Package Mechanical Data(SOT-23)

COMMON DIMENSIONS  
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.90	1.05	1.20
A1	0.00	0.05	0.10
A2	0.90	1.00	1.10
b	0.30	0.40	0.50
c	0.08	0.10	0.15
D	2.80	2.90	3.00
E	1.20	1.30	1.40
E1	2.30	2.40	2.50
L	0.30	0.40	0.50
θ	0°	5°	10°
L1	0.55 REF		
e	0.95 BSC		
e1	1.90 REF		

## Recommended Footprint



DIMENSIONS:MILLIMETERS

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

 is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.  
Copyright ©2023 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.