



## Description

### JMT N-channel Enhancement Mode Power MOSFET

#### Features

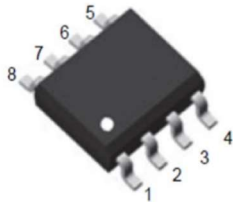
- 30V, 20A  
 $R_{DS(ON)} < 6m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 8.6m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

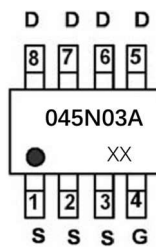
- Load Switch
- PWM Application
- Power management



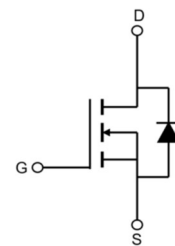
*100% UIS TESTED!*  
*100%  $\Delta V_{ds}$  TESTED!*



SOP-8 TOP View



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
045N03A	JMTP045N03A	TAPING	SOP-8	13inch	4000	48000

## Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ C$	20
		$T_A = 100^\circ C$	13
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	80	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	100	mJ
$P_D$	Power Dissipation	4	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	31.3	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.7	1.0	1.5	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note3</small>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	4.6	6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	6.1	8.6	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1.0MHz	-	1700	-	pF
C <sub>oss</sub>	Output Capacitance		-	320	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	300	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V	-	45	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	3	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	15	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =15V, I <sub>D</sub> =20A, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =10V	-	21	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	32	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	59	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	34	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	80	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, di/dt=100A/μs	-	15	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	4	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

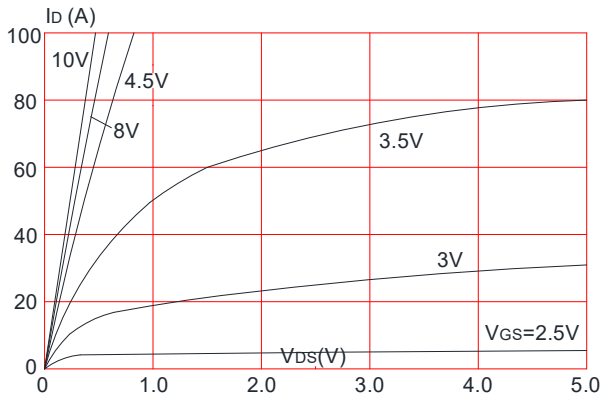
2. EAS condition: T<sub>J</sub>=25°C, V<sub>GS</sub>=15V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=20A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

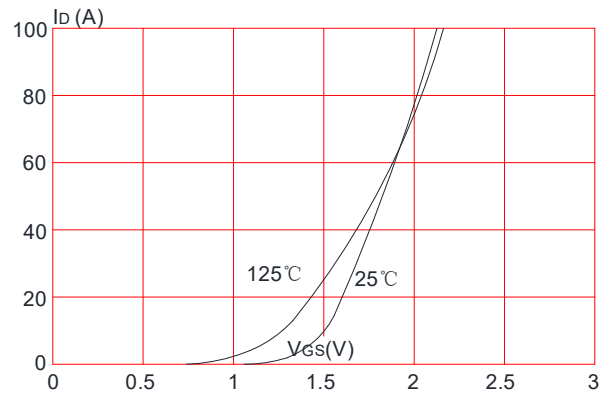


## Typical Performance Characteristics

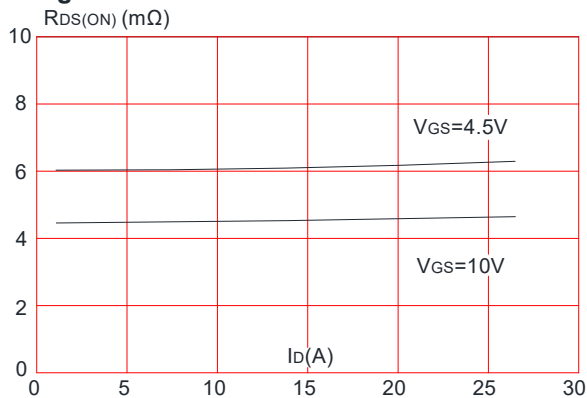
**Figure 1: Output Characteristics**



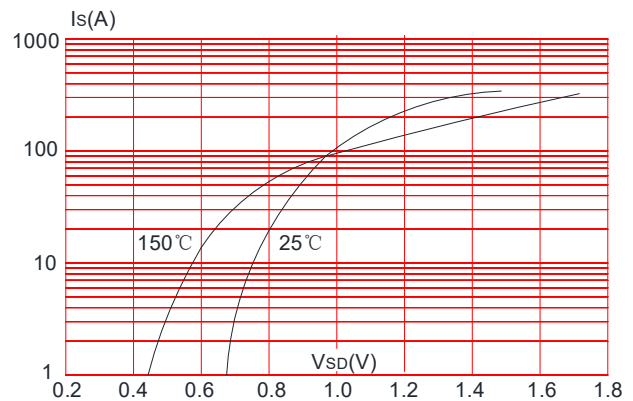
**Figure 2: Typical Transfer Characteristics**



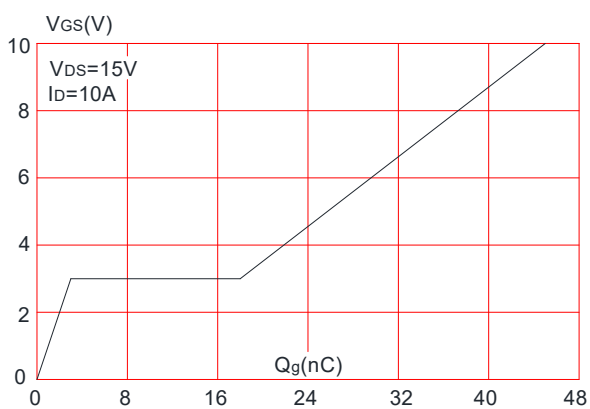
**Figure 3: On-resistance vs. Drain Current**



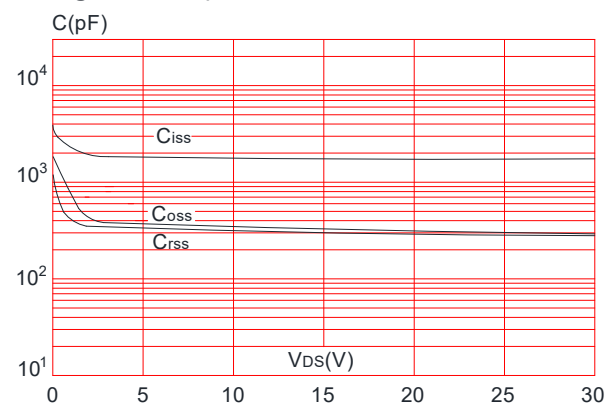
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**

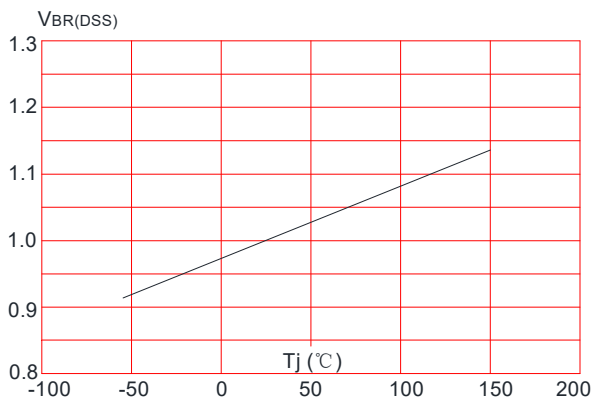


**Figure 6: Capacitance Characteristics**

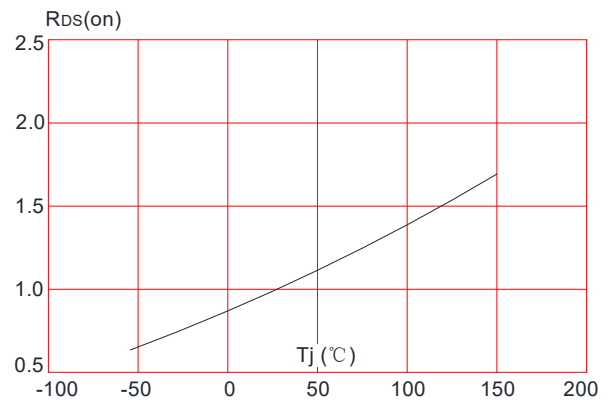




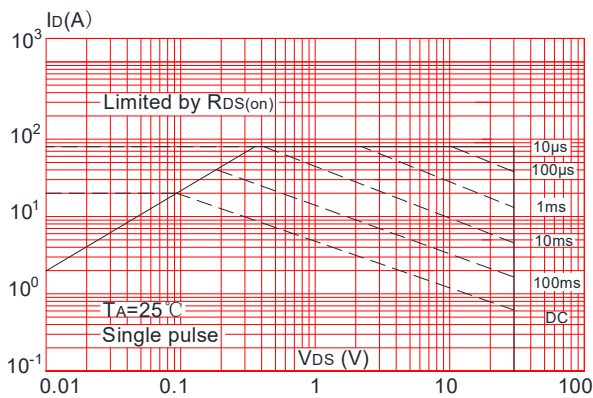
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



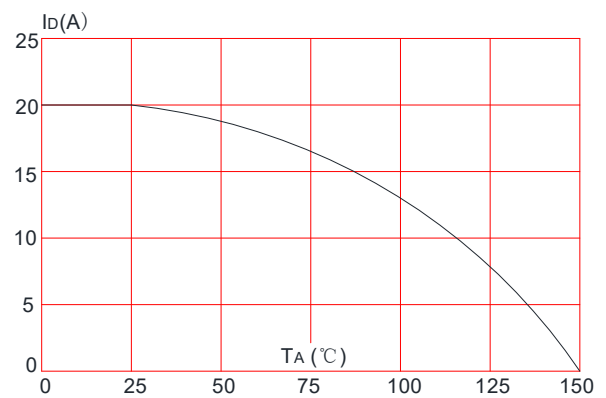
**Figure 8: Normalized on Resistance vs. Junction Temperature**



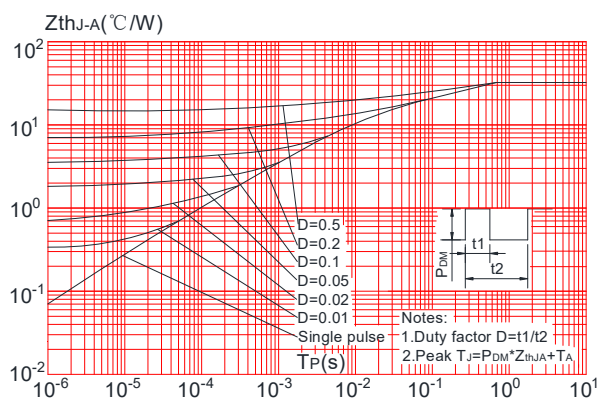
**Figure 9: Maximum Safe Operating Area**



**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**



## Test Circuit



Figure1:Gate Charge Test Circuit & Waveform

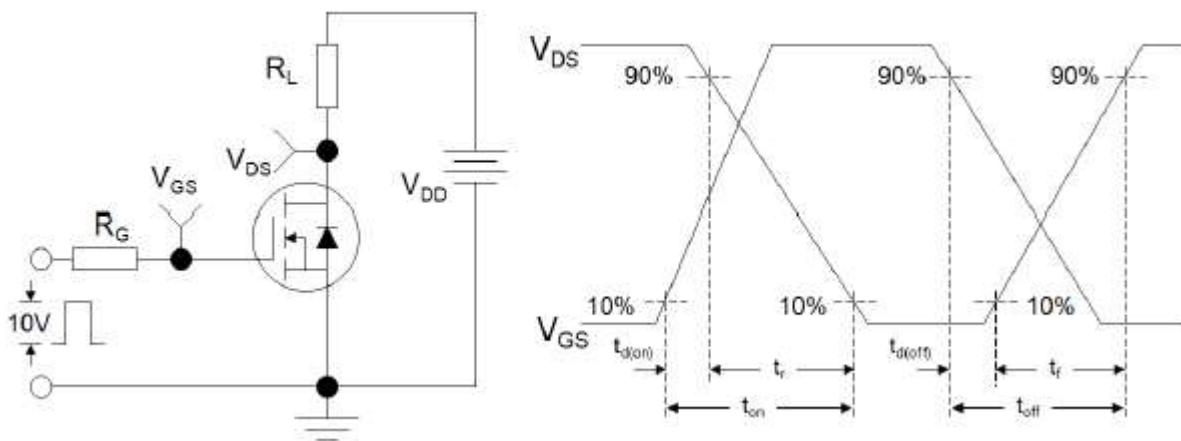


Figure 2: Resistive Switching Test Circuit & Waveforms

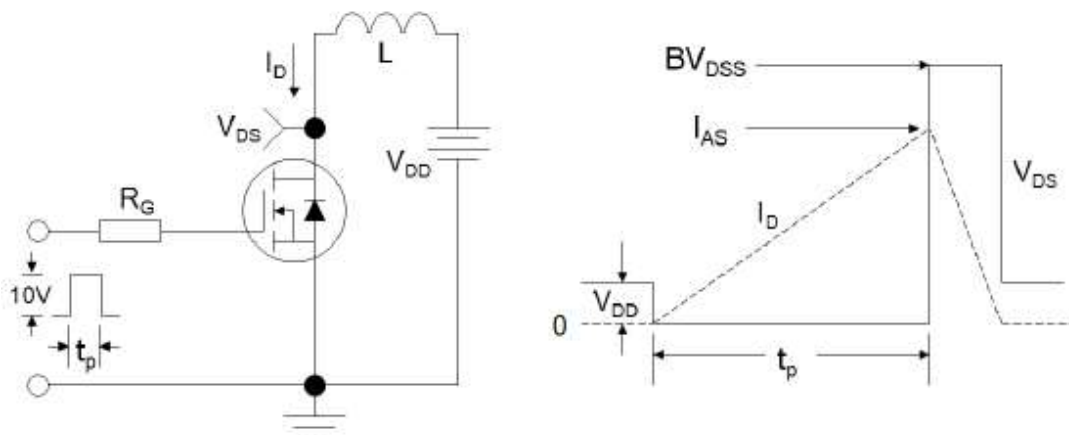
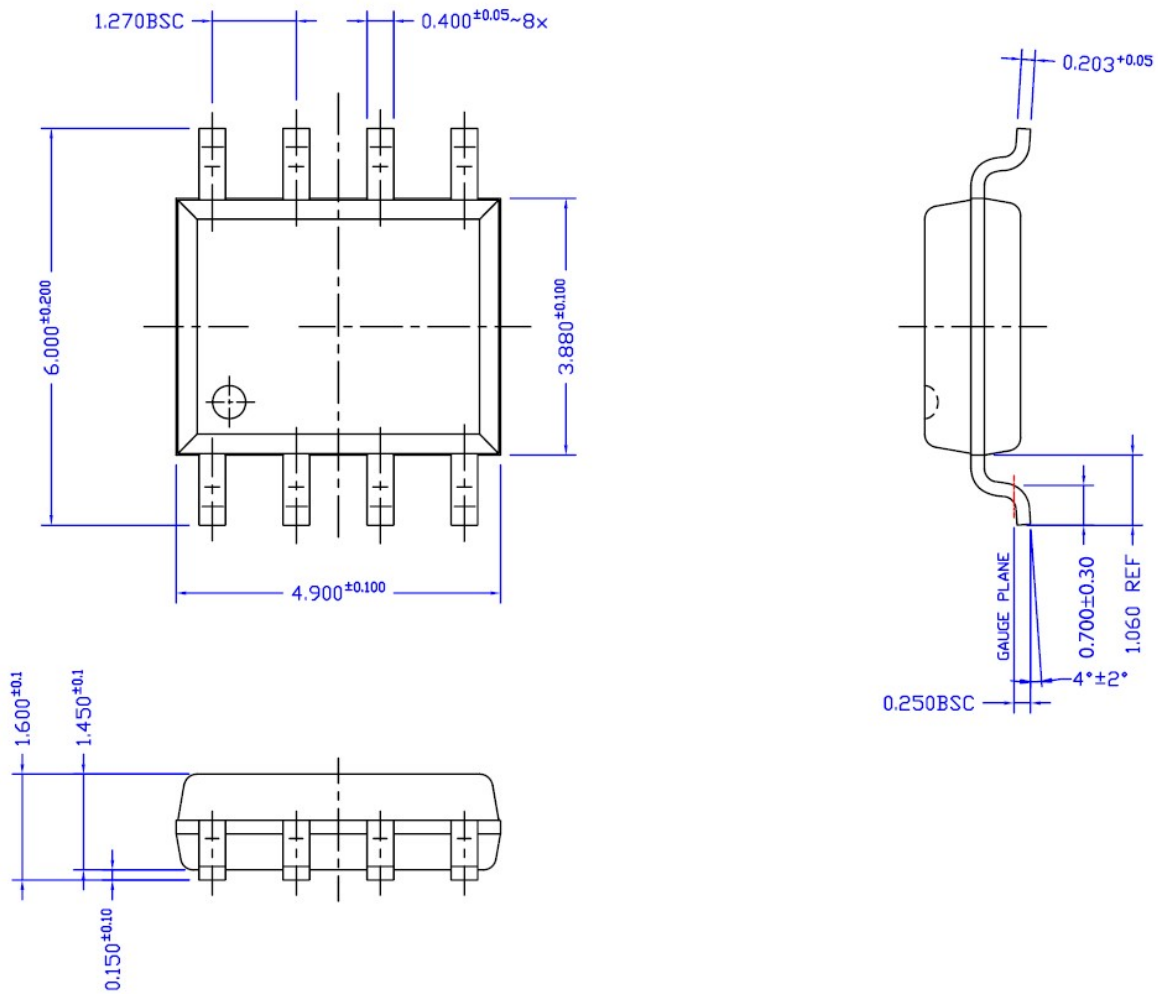


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data-SOP-8



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