



Description

JMT P-channel Enhancement Mode Power MOSFET

Features

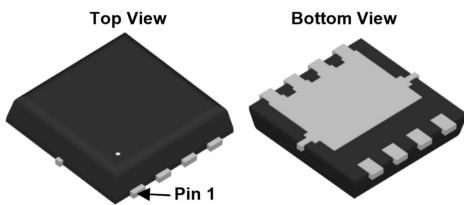
- $V_{DS} = -20V$, $I_D = -55A$
 $R_{DS(ON)} < 8.3m\Omega$ @ $V_{GS} = -4.5V$
 $R_{DS(ON)} < 10.4m\Omega$ @ $V_{GS} = -2.5V$
- High Power and Current Handling Capability
- Lead Free Product is Acquired
- Surface Mount Package

Application

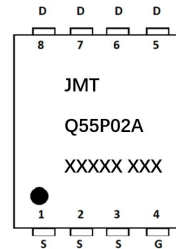
- PWM Applications
- Load Switch



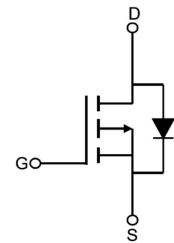
100% UIS TESTED!
100% ΔVds TESTED!



PDFN3x3-8L



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMTQ55P02A	JMTQ55P02A	TAPING	PDFN3x3-8L	13inch	5000	50000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	-55
		$T_C = 100^\circ C$	-35
I_{DM}	Pulsed Drain Current ^{note1}	-220	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	90	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	66
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.9	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-20	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V,	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.65	-1.0	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} =-4.5V, I _D =-15A	-	6.6	8.3	mΩ
		V _{GS} =-2.5V, I _D =-12A	-	8	10.4	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, f = 1.0MHz	-	4770	-	pF
C _{oss}	Output Capacitance		-	570	-	pF
C _{rss}	Reverse Transfer Capacitance		-	502	-	pF
Q _g	Total Gate Charge	V _{DS} =-10V, I _D =-15A, V _{GS} =-4.5V	-	56	-	nC
Q _{gs}	Gate-Source Charge		-	8	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	16	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-10V, I _D =-13A, R _{GEN} =2.7Ω, V _{GS} =-10V	-	11	-	ns
t _r	Turn-on Rise Time		-	110	-	ns
t _{d(off)}	Turn-off Delay Time		-	157	-	ns
t _f	Turn-off Fall Time		-	160	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-55	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-220	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S =-30A	-	-	-1.2	V
t _{rr}	Reverse Recovery Time	T _J =25°C, I _S =-15A,	-	23	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=-100A/μs	-	14	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25°C, V_{DD}=-10V, V_G=-10V, R_G=25Ω, L=0.5mH, I_{AS}=-19A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

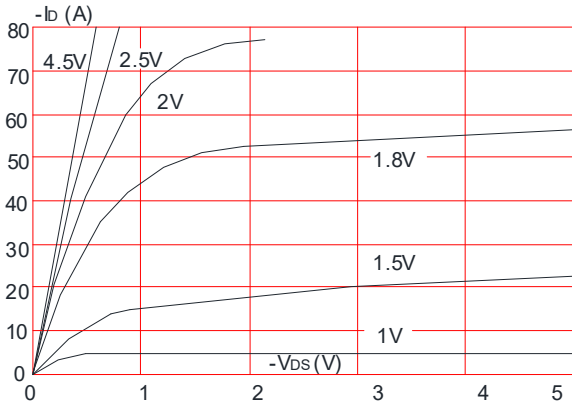


Figure 2: Typical Transfer Characteristics

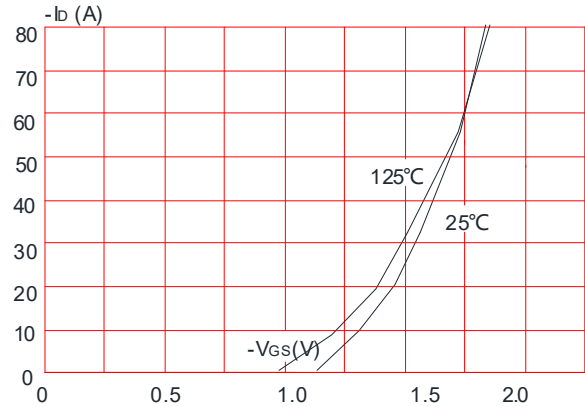


Figure 3: On-resistance vs. Drain Current

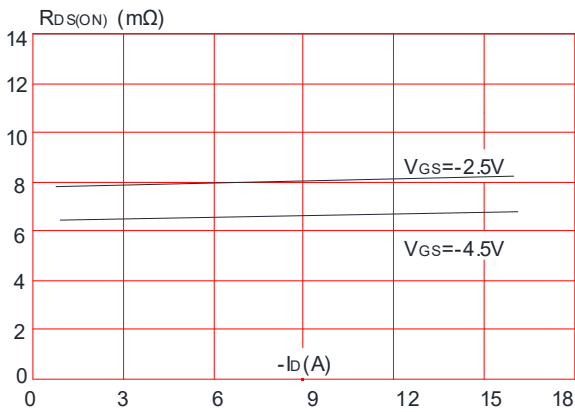


Figure 4: Body Diode Characteristics

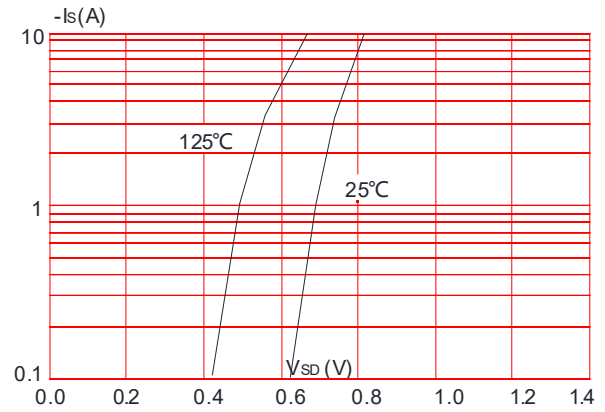


Figure 5: Gate Charge Characteristics

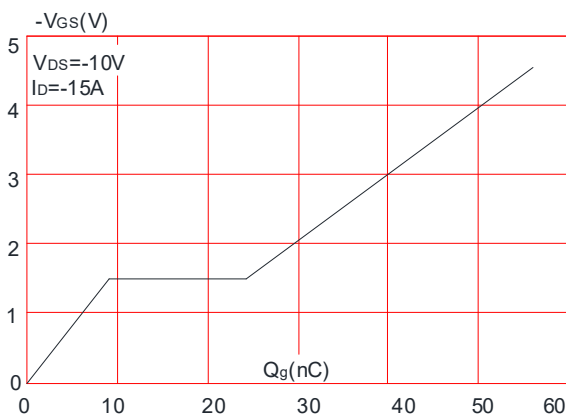


Figure 6: Capacitance Characteristics

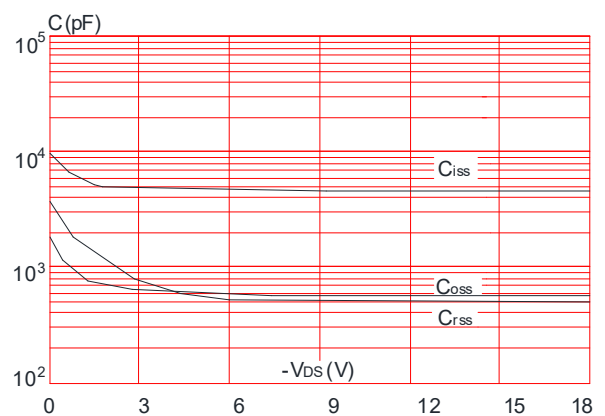




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

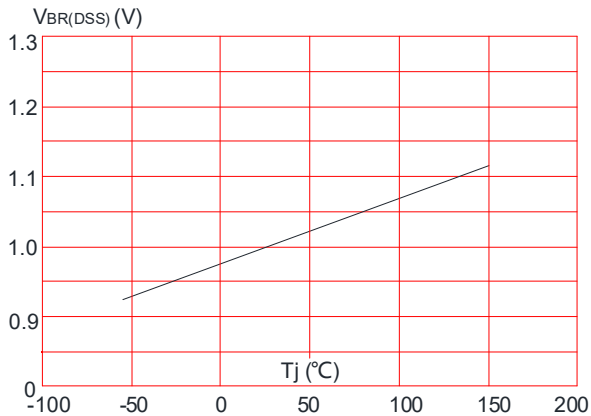


Figure 8: Normalized on Resistance vs. Junction Temperature

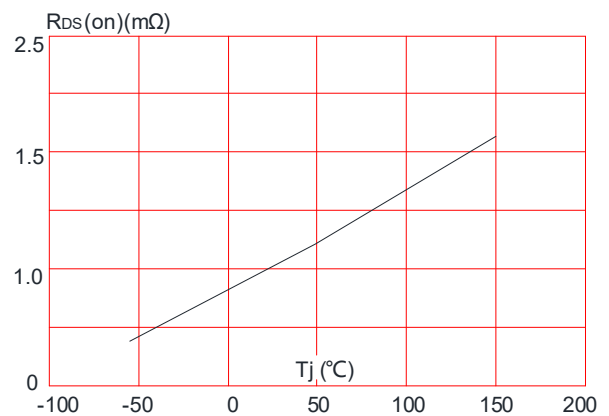


Figure 9: Maximum Safe Operating Area

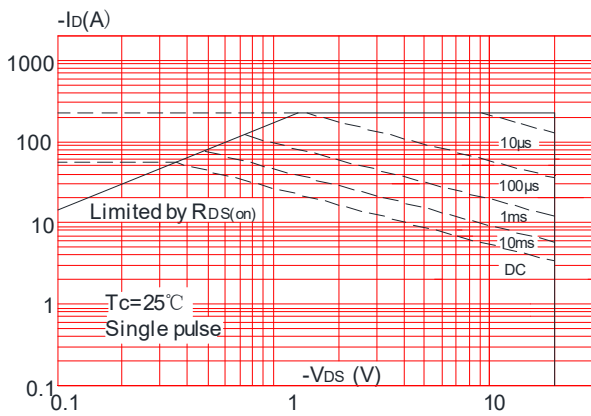


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

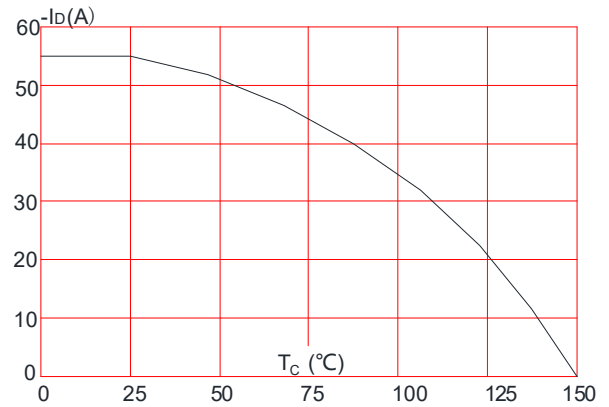
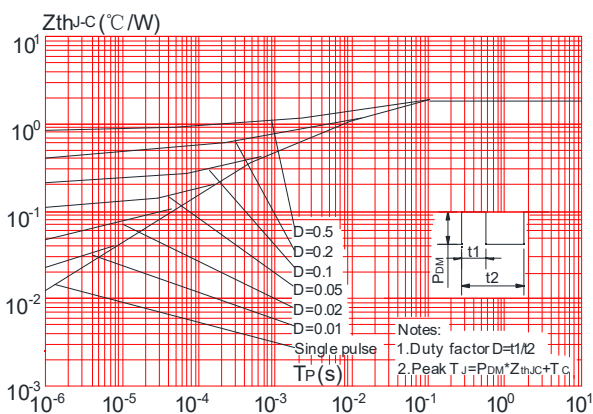
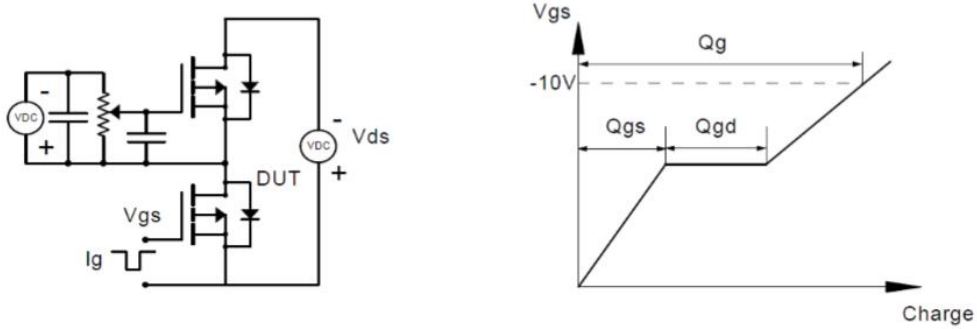


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

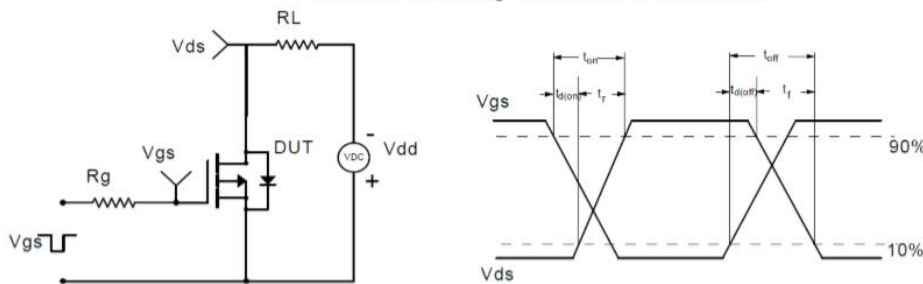


Test Circuit

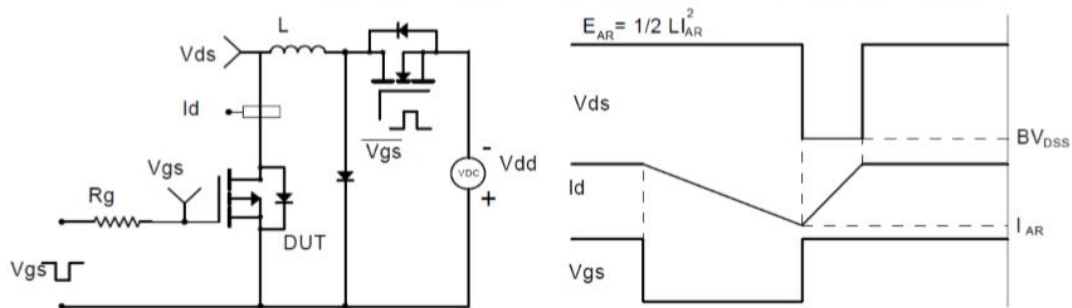
Gate Charge Test Circuit & Waveform



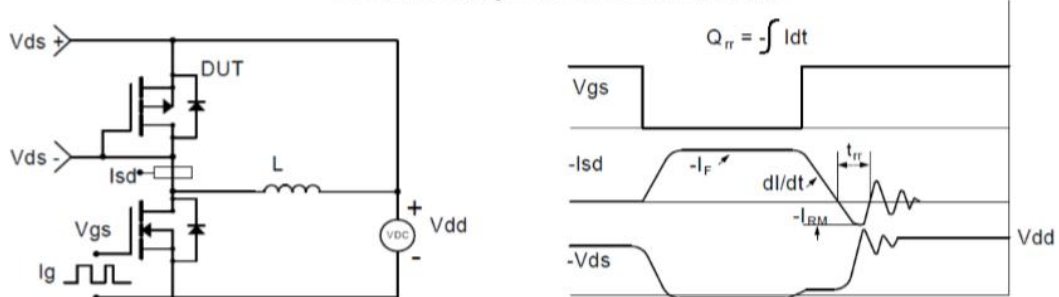
Resistive Switching Test Circuit & Waveforms



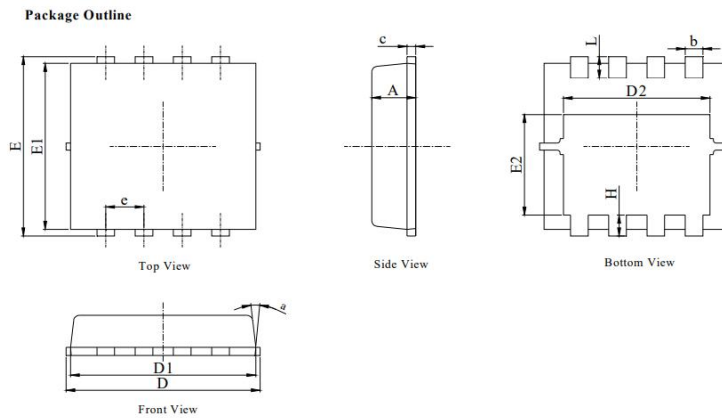
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN3x3-8L

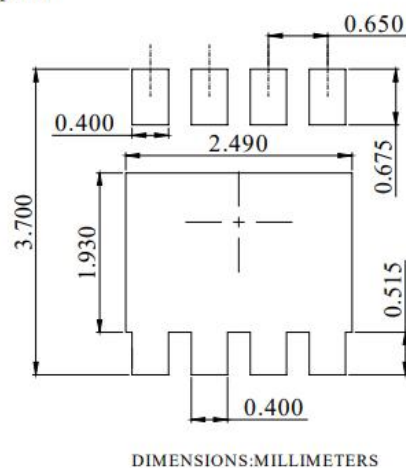


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°

Recommended Soldering Footprint





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