

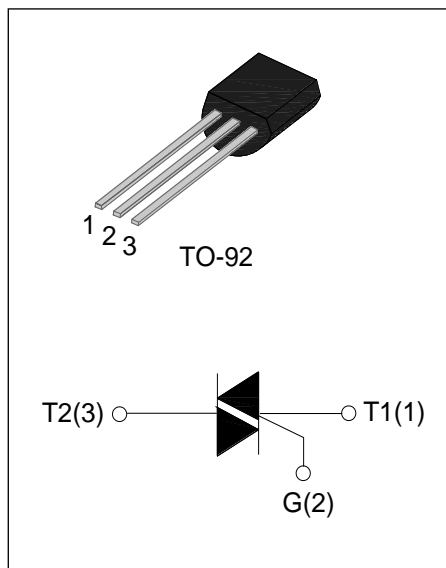


DESCRIPTION:

JST134CW series triacs with low holding and latching current are especially recommended for use on middle and small resistance type power load.

MAIN FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	4	A
V_{DRM}/V_{RRM}	800	V
I_{GT}	≤ 35	mA



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Storage junction temperature range		T_{stg}	-40 - 150	$^{\circ}C$
Operating junction temperature range		T_j	-40 - 125	$^{\circ}C$
Repetitive peak off-state voltage($T_j=25^{\circ}C$)		V_{DRM}	800	V
Repetitive peak reverse voltage($T_j=25^{\circ}C$)		V_{RRM}	800	V
Non repetitive surge peak Off-state voltage		V_{DSM}	$V_{DRM} + 100$	V
Non repetitive peak reverse voltage		V_{RSM}	$V_{RRM} + 100$	V
RMS on-state current	TO-92 ($T_C=90^{\circ}C$)	$I_{T(RMS)}$	4	A
Non repetitive surge peak on-state current (full cycle, $F=50Hz$)		I_{TSM}	25	A
I^2t value for fusing ($t_p=10ms$)		I^2t	3.1	A^2s
Critical rate of rise of on-state current ($I_G=2 \times I_{GT}$)	I - II - III	di/dt	50	A/ μs
	IV		10	
Peak gate current		I_{GM}	2	A
Average gate power dissipation		$P_{G(AV)}$	0.5	W
Peak gate power		P_{GM}	5	W

ELECTRICAL CHARACTERISTICS ($T_j=25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Test Condition	Quadrant		Value	Unit
I_{GT}	$V_D=12\text{V } R_L=33\Omega$	I - II -III	MAX	35	mA
V_{GT}		I - II -III	MAX	1.5	V
V_{GD}	$V_D=V_{DRM} T_j=125^{\circ}\text{C}$ $R_L=3.3\text{K}\Omega$	I - II -III	MIN	0.2	V
I_L	$I_G=1.2I_{GT}$	I -III	MAX	60	mA
		II		80	
I_H	$I_T=100\text{mA}$		MAX	60	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^{\circ}\text{C}$		MIN	500	V/ μs
(dV/dt)c	(dI/dt)c=1.1A/ms $T_j=125^{\circ}\text{C}$		MIN	10	V/ μs

STATIC CHARACTERISTICS

Symbol	Parameter		Value(MAX)	Unit
V_{TM}	$I_{TM}=5\text{A } t_p=380\mu\text{s}$	$T_j=25^{\circ}\text{C}$	1.7	V
I_{DRM}	$V_D=V_{DRM} V_R=V_{RRM}$	$T_j=25^{\circ}\text{C}$	5	μA
I_{RRM}		$T_j=125^{\circ}\text{C}$	1	mA

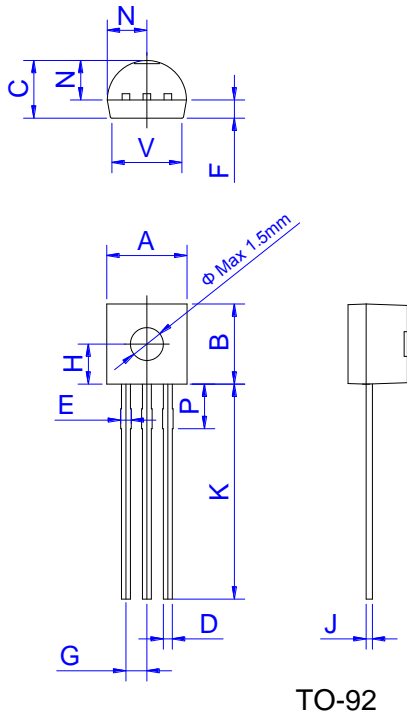
THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	junction to case(AC)	TO-92	7.9	$^{\circ}\text{C/W}$

ORDERING INFORMATION

<p>J</p> <p>JieJie Microelectronics Co.,Ltd</p>	<p>ST</p> <p>Triacs</p>	<p>134</p> <p>$I_{T(RMS)}:4\text{A}$</p>	<p>U</p> <p>U:TO-92</p>	<p>-800</p> <p>$800:V_{DRM} / V_{RRM} \geq 800\text{V}$</p>	<p>CW</p> <p>CW: $I_{GT1-3} \leq 35\text{mA}$</p>
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PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.45		5.20	0.175		0.205
B	4.32		5.33	0.170		0.210
C	3.18		4.19	0.125		0.165
D	0.407		0.533	0.016		0.021
E	0.60		0.80	0.024		0.031
F	-	1.1	-	-	0.043	-
G	-	1.27	-	-	0.050	-
H	-	2.30	-	-	0.091	-
J	0.36		0.50	0.014		0.020
K	12.70		15.0	0.500		0.591
N	2.04		2.66	0.080		0.105
P	1.86		2.06	0.073		0.081
V	-		4.3	-		0.169

FIG.1: Maximum power dissipation versus RMS on-state current

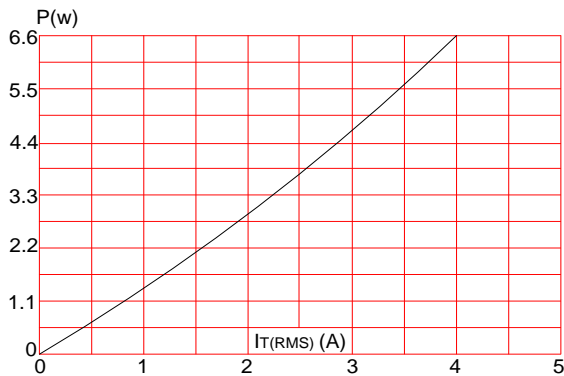


FIG.2: RMS on-state current versus case temperature

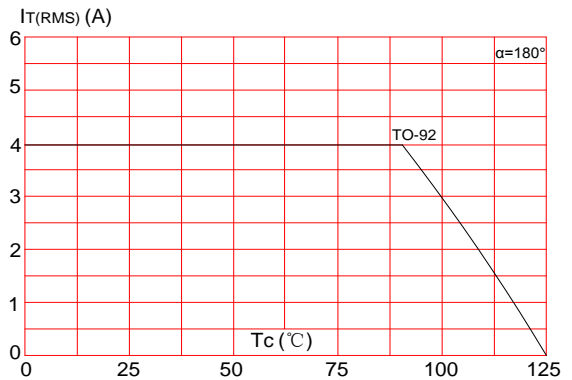


FIG.3: Surge peak on-state current versus number of cycles

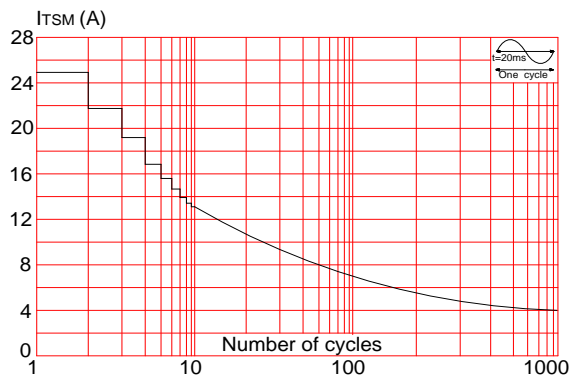


FIG.4: On-state characteristics (maximum values)

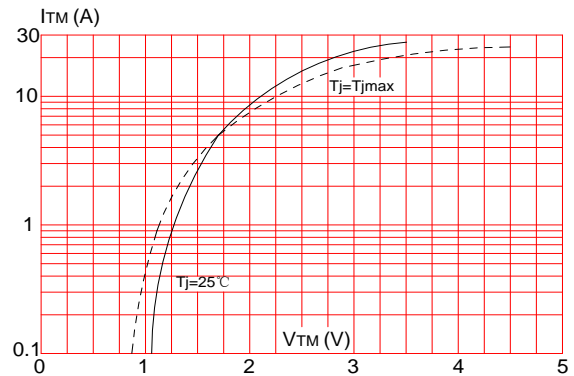


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$ and corresponding value of I^2t ($I_{\text{I-III}}:di/dt < 50\text{A}/\mu\text{s}$; $I_{\text{IV}}:di/dt < 10\text{A}/\mu\text{s}$)

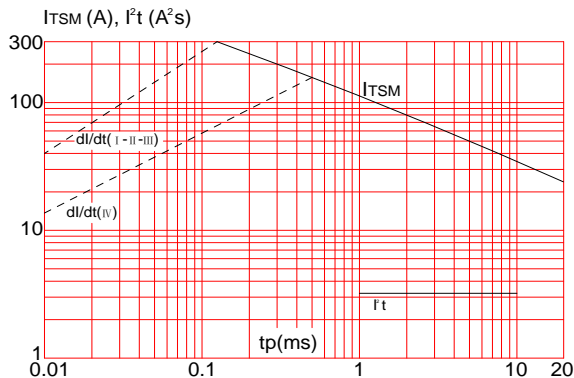


FIG.7: Relative variations of holding current versus junction temperature

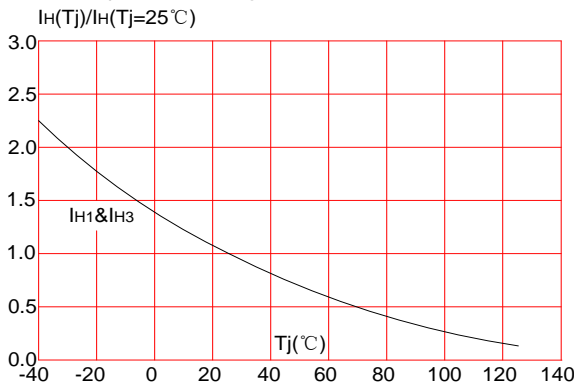


FIG.6: Relative variations of gate trigger current versus junction temperature

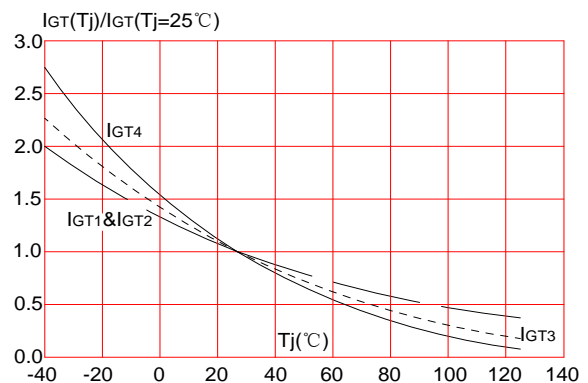
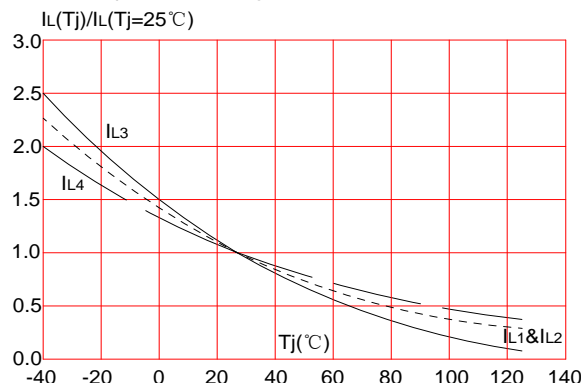



FIG.8: Relative variations of latching current versus junction temperature



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