



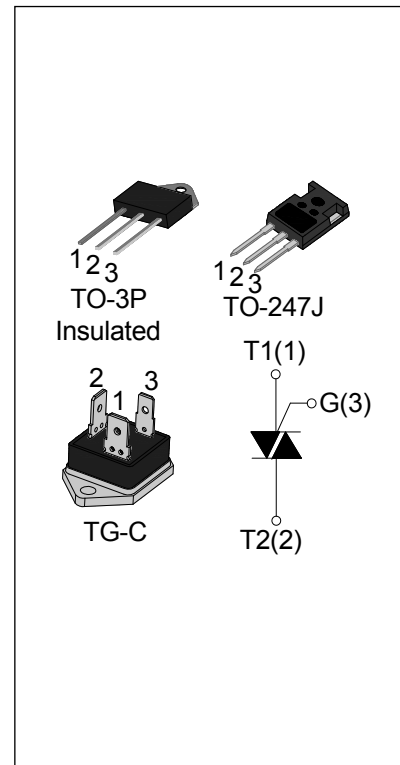
DESCRIPTION:

With high ability to withstand the shock loading of large current, JST41 series triacs provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrants products especially recommended for use on inductive load.

From all three terminals to external heatsink, JST41Z provides a rated insulation voltage of 2500 V_{RMS}, complying with UL standards (File ref: E252906).

MAIN FEATURES

Symbol	Value	Unit
I _{T(RMS)}	40	A
V _{DRM} /V _{RRM}	600/800/1200/1600	V



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Storage junction temperature range		T _{stg}	-40-150	°C
Operating junction temperature range		T _j	-40-125	°C
Repetitive peak off-state voltage (T _j =25°C)		V _{DRM}	600/800/1200/1600	V
Repetitive peak reverse voltage (T _j =25°C)		V _{RRM}	600/800/1200/1600	V
Non repetitive peak off-state voltage		V _{DSM}	V _{DRM} +100	V
Non repetitive peak reverse voltage		V _{RSM}	V _{RRM} +100	V
RMS on-state current	TO-3P(Ins) (T _c =80°C)	I _{T(RMS)}	40	A
	TO-247J/ TG-C (T _c =90°C)			
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I _{TSM}	400	A
I ² t value for fusing (tp=10ms)		I ² t	880	A ² s
Critical rate of rise of on-state current (I _G =2 × I _{GT})		dI/dt	50	A/μs

Peak gate current	I_{GM}	4	A
Average gate power dissipation	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	10	W

ELECTRICAL CHARACTERISTICS ($T_j=25^\circ\text{C}$ unless otherwise specified)

3 Quadrants

Symbol	Test Condition	Quadrant		Value		Unit
				BW	CW	
I_{GT}	$V_D=12\text{V } R_L=33\Omega$	I - II -III	MAX	50	35	mA
V_{GT}		I - II -III	MAX	1.3		V
V_{GD}	$V_D=V_{DRM} T_j=125^\circ\text{C}$ $R_L=3.3\text{K}\Omega$	I - II -III	MIN	0.2		V
I_L	$I_G=1.2I_{GT}$	I -III	MAX	80	70	mA
		II		100	80	
I_H	$I_T=100\text{mA}$		MAX	60	50	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^\circ\text{C}$		MIN	1500	1000	V/ μs

4 Quadrants

Symbol	Test Condition	Quadrant		Value	Unit
I_{GT}	$V_D=12\text{V } R_L=33\Omega$	I - II -III	MAX	50	mA
		IV		70	
V_{GT}		ALL	MAX	1.3	V
V_{GD}	$V_D=V_{DRM} T_j=125^\circ\text{C}$ $R_L=3.3\text{K}\Omega$	ALL	MIN	0.2	V
I_L	$I_G=1.2I_{GT}$	I -III-IV	MAX	90	mA
		II		100	
I_H	$I_T=100\text{mA}$		MAX	80	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^\circ\text{C}$		MIN	1000	V/ μs

STATIC CHARACTERISTICS

Symbol	Parameter		Value(MAX)	Unit
V_{TM}	$I_{TM}=60A$ $t_p=380\mu s$	$T_j=25^\circ C$	1.5	V
I_{DRM}	$V_D=V_{DRM}$ $V_R=V_{RRM}$	$T_j=25^\circ C$	10	μA
I_{RRM}		$T_j=125^\circ C$	5	mA

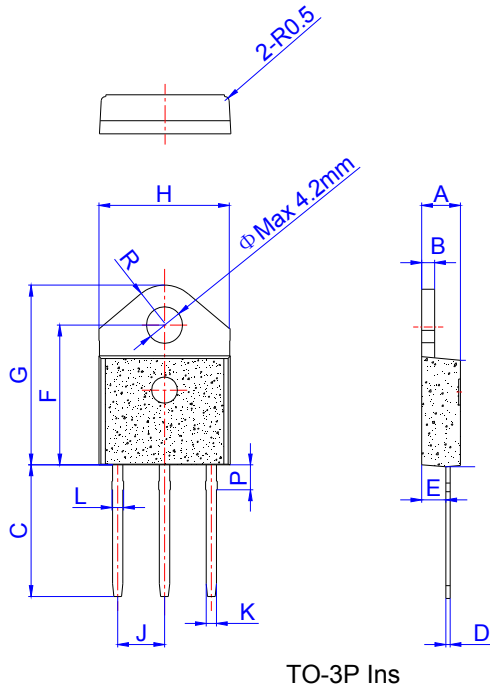
THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	junction to case(AC)	TO-3P(Ins)	1.1	$^\circ C/W$
		TG-C	0.65	
		TO-247J	0.9	

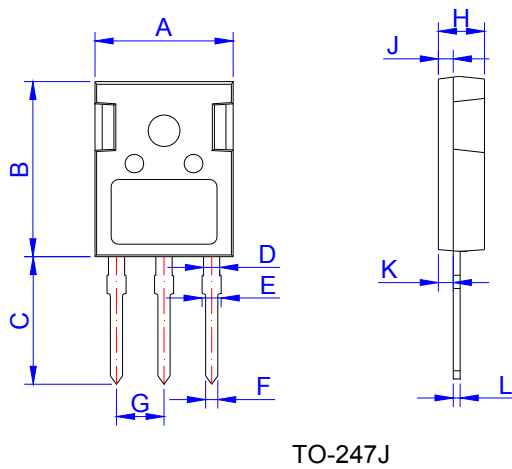
ORDERING INFORMATION

<p>JieJie Microelectronics Co.,Ltd</p>	<p>J</p> <p>Triacs</p> <p>$I_{T(RMS)}:40A$</p> <p>Z:TO-3P(Ins) SJ:TO-247J T:TG-C</p>	<p>ST</p>	<p>41</p>	<p>Z</p>	<p>-600</p> <p>600:$V_{DRM}/V_{RRM} \geq 600V$ 800:$V_{DRM}/V_{RRM} \geq 800V$ 1200:$V_{DRM}/V_{RRM} \geq 1200V$ 1600:$V_{DRM}/V_{RRM} \geq 1600V$</p>	<p>BW</p> <p>CW:$I_{GT1-3} \leq 35mA$ BW:$I_{GT1-3} \leq 50mA$ B:$I_{GT1-3} \leq 50mA$ $I_{GT4} \leq 70mA$</p>
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PACKAGE MECHANICAL DATA

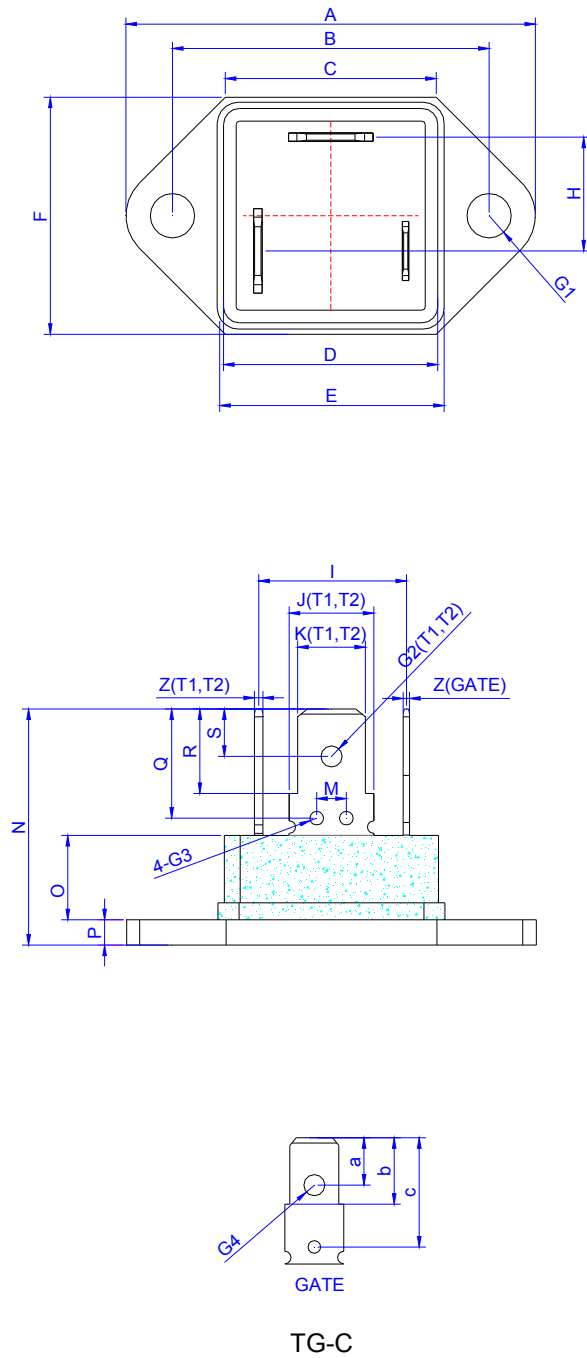


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.50		0.70	0.020		0.028
E	2.70		2.90	0.106		0.114
F	15.80		16.50	0.622		0.650
G	20.40		21.10	0.803		0.831
H	15.10		15.50	0.594		0.610
J	5.40		5.65	0.213		0.222
K	1.10		1.40	0.043		0.055
L	1.35		1.50	0.053		0.059
P	2.80		3.00	0.110		0.118
R		4.35			0.171	



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.50	15.80	16.10	0.610	0.622	0.634
B	20.80	21.00	22.20	0.819	0.828	0.874
C	19.70	20.00	20.30	0.776	0.787	0.799
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.90	2.10	2.30	0.075	0.083	0.091
F	1.00	1.20	1.40	0.039	0.047	0.055
G		5.44			0.214	
H	4.80	5.00	5.20	0.189	0.197	0.205
J	1.90	2.00	2.10	0.075	0.079	0.083
K	2.20	2.35	2.50	0.087	0.093	0.098
L	0.41	0.60	0.79	0.016	0.024	0.031

PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			39.2			1.543
B	29.8	30.0	30.2	1.173	1.181	1.189
C			20.2			0.795
D			20.5			0.807
E			21.6			0.85
F			23			0.905
G1	Φ4.1	Φ4.2	Φ4.3	Φ0.161	Φ0.165	Φ0.169
H		10.3			0.406	
I		13.9			0.547	
J(T1,T2)		8			0.315	
K(T1,T2)		6.4			0.252	
M	2.7	3.0	3.3	0.106	0.118	0.130
N			22.8			0.898
O		8.2			0.323	
P		2.5			0.098	
Q	9.45	9.75	10.1	0.374	0.383	0.398
R	7.8	7.95	8.1	0.307	0.313	0.319
S	4.3	4.5	4.7	0.169	0.177	0.185
Z(T1,T2)	0.78	0.8	0.85	0.0307	0.0315	0.0335
G2(T1,T2)		Φ2	Φ2.2		Φ0.079	Φ0.087
G3	Φ1.1	Φ1.3	Φ1.5	Φ0.043	Φ0.051	Φ0.059
G4		Φ1.55	Φ1.75		Φ0.061	Φ0.069
a	2.95	3.15	3.35	0.116	0.124	0.132
b	6.2	6.35	6.5	0.244	0.25	0.256
c	9.35	9.75	10	0.368	0.384	0.393
Z(GATE)	0.58	0.6	0.65	0.0228	0.0236	0.0256
J(GATE)		5.6			0.221	
K(GATE)		4.65			0.183	

FIG.1 Maximum power dissipation versus RMS on-state current

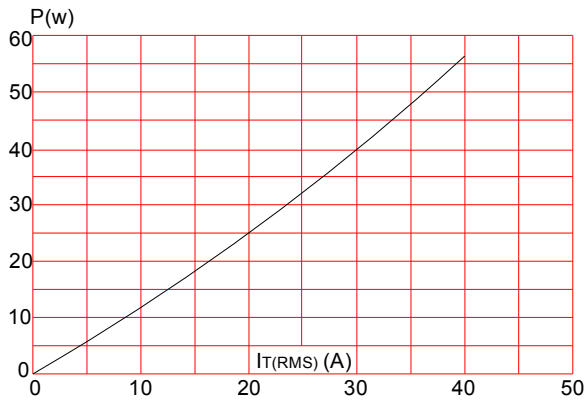


FIG.3: Surge peak on-state current versus number of cycles

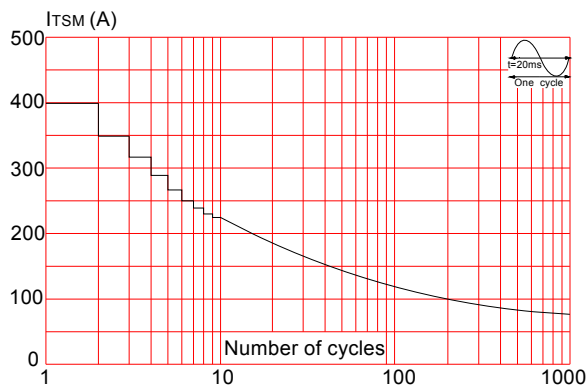


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of I^2t ($di/dt < 50\text{A}/\mu\text{s}$)

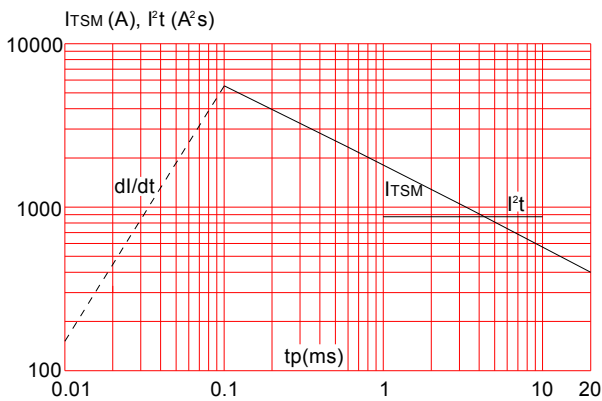


FIG.2: RMS on-state current versus case temperature

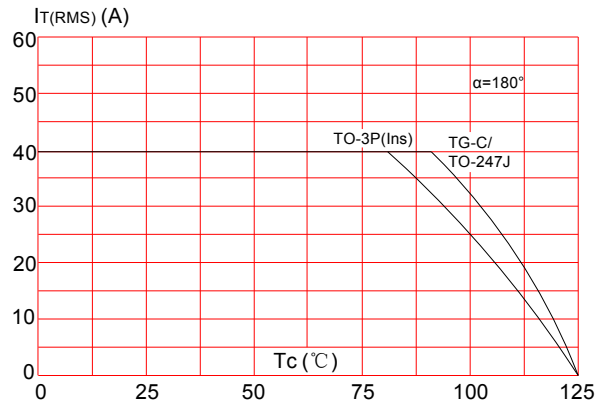


FIG.4: On-state characteristics (maximum values)

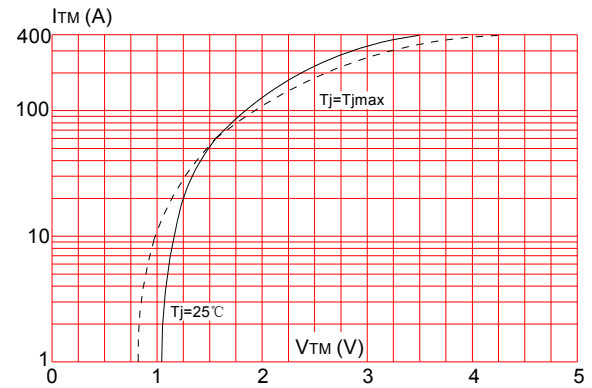
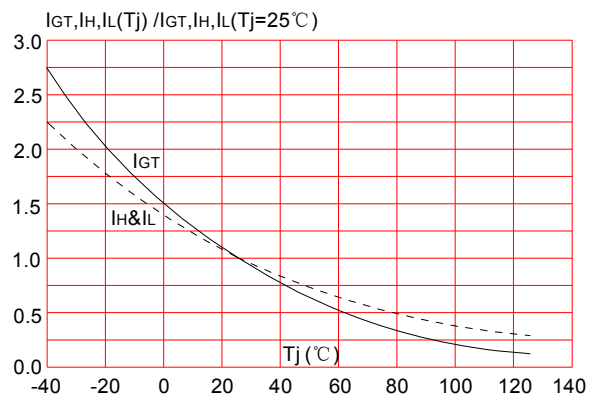



FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



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