



JMT320KH18T3

Thyristor Module

Features

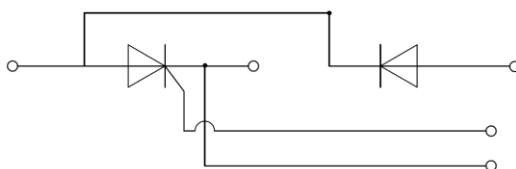
- Half-bridge SCR configuration integrated in a single package
- With high thermal conductivity DBC as the Insulation
- Welding by vacuum welding technology, which provide high reliability

Product Summary

Parameter	Value	Unit
V_{RRM}	1800	V
$I_{T(AV)}(@ T_C = 85^{\circ}C)$	320	A
$I_{TSM}(@ t_p = 10ms)$	9500	A
$V_T(Max)$	1.80	V

Applications

- Temperature control
- Light control system
- DC motor



Absolute Maximum Ratings (@ $T_C = 25^{\circ}C$ unless otherwise specified)

Parameter	Conditions	Symbol	Values	Unit
Repetitive peak off-state voltage	$T_{vj} = 25^{\circ}C$	V_{DRM}	1800	V
Repetitive peak reverse voltage	$T_{vj} = 25^{\circ}C$	V_{RRM}	1800	V
Non-repetitive peak off-state voltage	$T_{vj} = 25^{\circ}C$	V_{DSM}	1900	V
Non-repetitive peak reverse voltage	$T_{vj} = 25^{\circ}C$	V_{RSM}	1900	V
Average forward current	$T_C = 85^{\circ}C$	$I_{T(AV)}$	320	A
Forward surge current	1/2 cycle, Sine wave, 50Hz $T_{vj} = 25^{\circ}C$	I_{TSM}	9500	A
I^2t value for fusing		I^2t	450000	A^2s
Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$	di/dt	150	$A/\mu s$
RMS isolation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000	V
Junction temperature range		T_J	-40 ~ +125	$^{\circ}C$
Storage temperature range		T_{stg}	-40 ~ +125	$^{\circ}C$

**Electrical Characteristics (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)**

Parameter	Conditions	Symbol	Values			Unit
			Min.	Typ.	Max.	
Peak forward voltage	$I_T=960\text{A}$, $t_P=380\mu\text{s}$	V_T			1.80	V
Repetitive peak off-state current	$V_D = V_{\text{DRM}}$, $T_{vj} = 25^\circ\text{C}$	I_{DRM}			100	μA
	$V_D = V_{\text{DRM}}$, $T_{vj} = 125^\circ\text{C}$				100	mA
Reverse leakage current	$V_R = V_{\text{RRM}}$, $T_{vj} = 25^\circ\text{C}$	I_{RRM}			100	μA
	$V_R = V_{\text{RRM}}$, $T_{vj} = 125^\circ\text{C}$				100	mA
Threshold voltage	For power loss calculation only $T_{vj} = 125^\circ\text{C}$,	V_{TO}			0.78	V
Dynamic resistance	$T_{vj} = 125^\circ\text{C}$,	r_T			0.8	$\text{m}\Omega$
Triggering gate current	$V_D=12\text{V}$ $R_L=30\Omega$	I_{GT}	20		150	mA
Holding current	$I_T=1\text{A}$	I_H			300	mA
Latching current	$I_G=1.2 I_{\text{GT}}$	I_L			400	mA
Triggering gate voltage	$V_D=12\text{V}$ $R_L=30\Omega$	V_{GT}			1.8	V
Non triggering gate voltage	$V_D=0.5V_{\text{DRM}}$ $T_{vj}=125^\circ\text{C}$	V_{GD}			0.25	V

Thermal Characteristics (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Values			Unit
			Min.	Typ.	Max.	
Thermal resistance, junction to case	per chip	$R_{\text{th(j-c)}}$		0.09		$^\circ\text{C/W}$
Thermal resistance, case to heatsink	per chip	$R_{\text{th(c-s)}}$		0.05		$^\circ\text{C/W}$
Mounting torque	Module and heatsink fixed torque M5	M	4.25		5.75	$\text{N}\cdot\text{m}$
	Electrode connection torque M8		7.65		10.34	$\text{N}\cdot\text{m}$



Ordering Information

Device	Marking	Package	Weight	Inner Box	Per Carton
JMT320KH18T3	JMT320KH18T3	T3	355±10g/PCS	3 PCS	27 PCS

Typical Electrical & Thermal Characteristics

FIG.1:Power dissipation vs. on-state current
(per thyristor or diode)

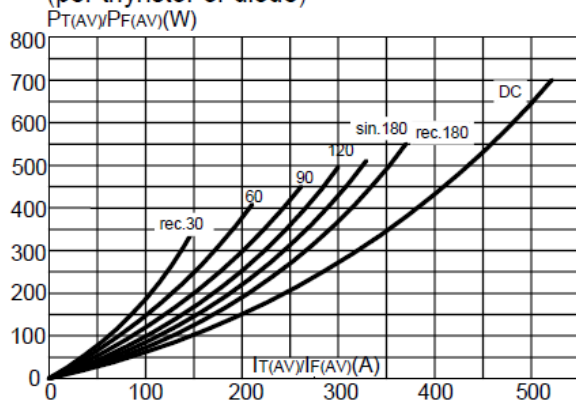


FIG.2: Maximum transient thermal impedance
junction to case(per thyristor or diode)

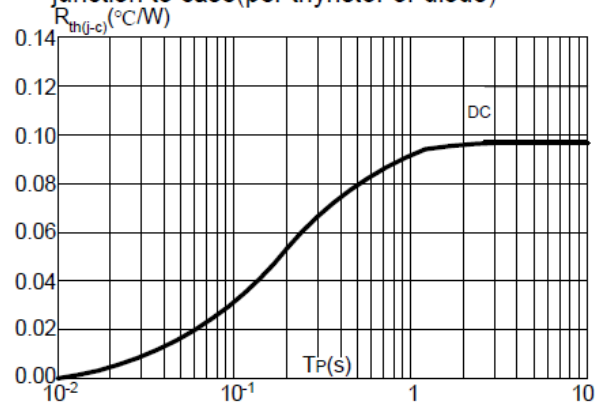


FIG.3:Forward characteristics
(per thyristor or diode)

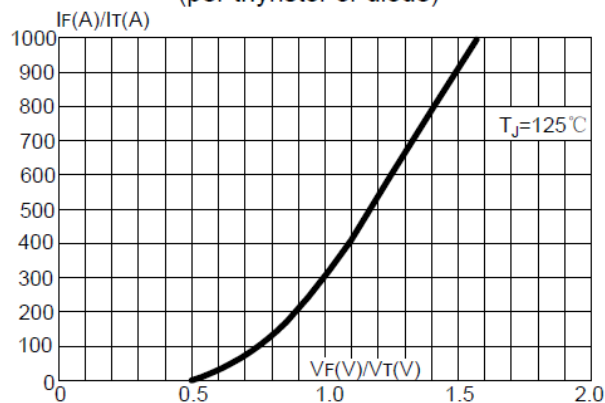


FIG.4: Relative variations of gate trigger current, holding current and latching current versus junction temperature

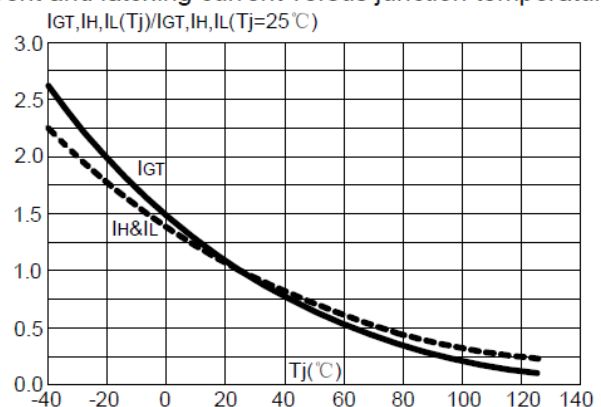


FIG.5 Gate trigger characteristics

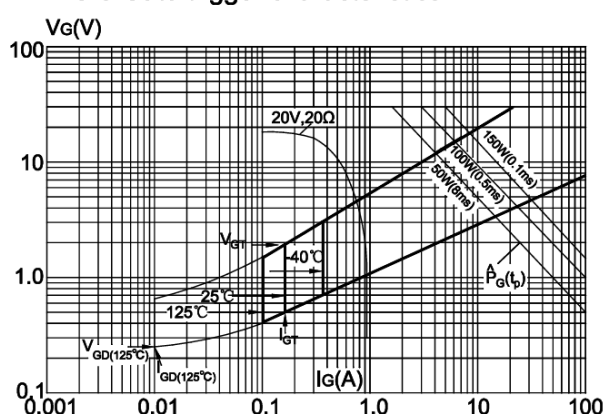
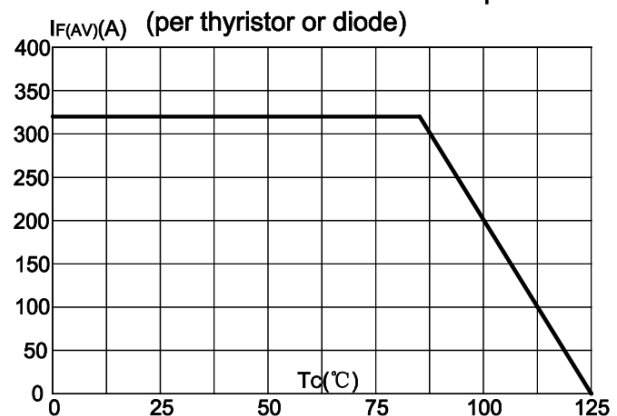
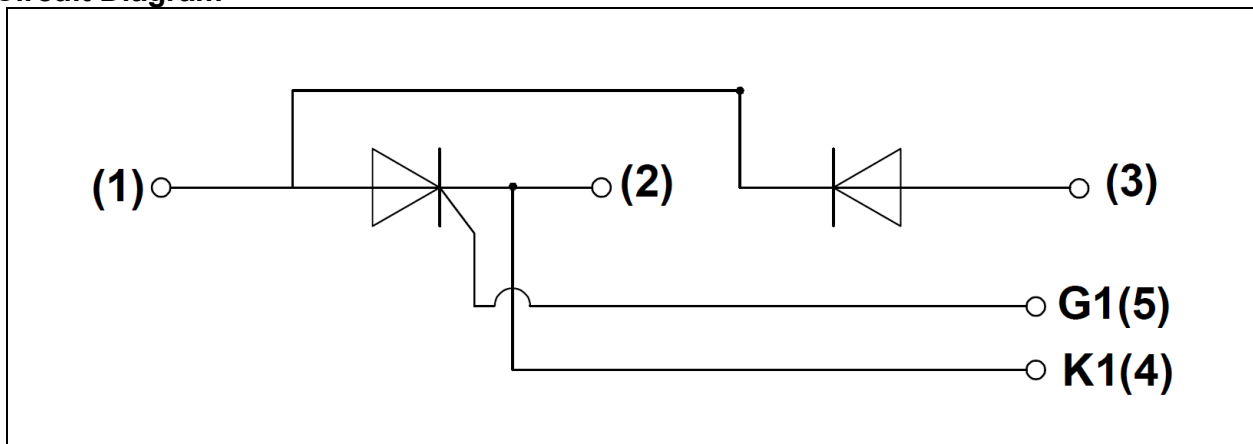
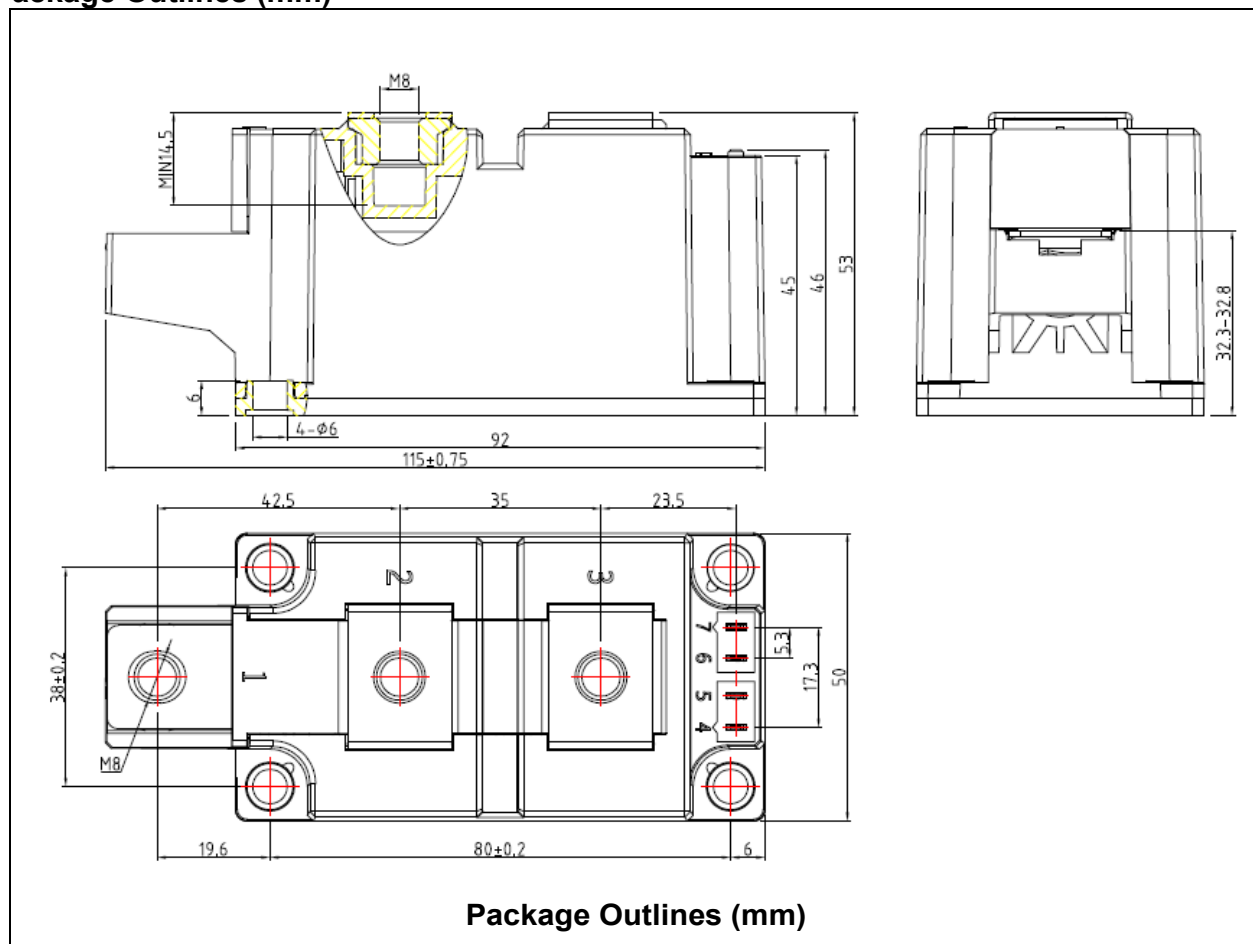


FIG.6: Forward current vs. case temperature



Circuit Diagram

Package Outlines (mm)




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